A HIGH-SPEED TWO-STEP ANALOG-TO-DIGITAL CONVERTER WITH AN OPEN-LOOP RESIDUE AMPLIFIER

A Thesis
Presented to
The Academic Faculty

by

Hüseyin Dinç

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
May 2011

A HIGH-SPEED TWO-STEP ANALOG-TO-DIGITAL CONVERTER WITH AN OPEN-LOOP RESIDUE AMPLIFIER

Approved by:

Professor Phillip E. Allen, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Maysam Ghovanloo
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Paul E. Hasler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Pamela Bhatti
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor David Anderson
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Levent Değertekin
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: April 2011

To my parents.

ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisors Dr. Allen and Dr. Hasler for their guidance and support through out my Ph.D. education. I would like to thank Texas Instruments (TI) for the financial support I received through the TI Analog Student Fellowship Program. I extend my appreciation to National Semiconductor Company (NSC) for fabricating my prototype ICs and allowing me use their simulation tools and test equipment. Patrick O'Farrell and Arlo Aude of NSC have helped me improve my design and professionalism by providing feedback during my design reviews and through many discussions. They have been very patient with me and helped me in many ways. Their mentorship was invaluable. My gratitude to them cannot be expressed in words. I am also grateful to Oguz Altun for being my TI mentor. Many discussions with my friends Pooya Forghani-zadeh, Luke Milner, Susanta Sengupta, Erhan Ozalevli, Vishal Gupta, and Ajay Kumar improved my understanding of analog IC design. I express my appreciation to them. I would like to thank my wife for her care and support. I especially thank her for proofreading my thesis and improving my writing. Last but not least, I am grateful to my family for their support and encouragement.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

With the revolution of the digital CMOS design, the CMOS technology has become the dominant process technology in today's semiconductor industry. However, as the channel lengths of the MOS transistors reduce with the introduction of each CMOS process node, the intrinsic gain (gm $\times$ rds) of the MOS transistors decreases. As this trend continues, the high-gain amplifiers required for accurate residue amplification in pipelined ADCs will not have enough open-loop gain to provide sufficient accuracy. Therefore, achievable accuracy or speed must be lowered. On the other hand, new circuit architectures and clever use of the readily available powerful DSP capability can be exploited to decouple the gain, accuracy, and speed requirements.

The main objective of this research was to develop a background calibration technique that would enable the design of a 2-stage pipelined ADC with an open-loop residue amplifier. This technique and its variations can potentially eliminate the need for high-gain amplifiers in pipelined ADCs, which is especially vital for high-performance ADC design in modern fine-line CMOS technologies.

Moreover, a double-switching switched-buffer SHA architecture was proposed and demonstrated. The proposed double-switching architecture eliminates the hold-mode feed-through. Therefore, the SHA maintains its linearity with input frequencies as high as the Nyquist rate.

CHAPTER I

INTRODUCTION

Silicon complementary-metal-oxide-semiconductor (CMOS) process technology has been evolving for decades as predicted by Gordon Moore. As CMOS processes matured with aggressive transistor scaling, their high-frequency performance and integration density improved tremendously. The improvements in CMOS processes led to vast design possibilities and advances in digital circuit design, which resulted in area- and power-efficient realizations of very complex digital-signal-processing (DSP) algorithms and functions with relative ease. However, analog circuit design, as a result analog signal processing (ASP), could not exploit the improvements in CMOS technology as much as digital circuit design. Further, because of its distinct advantages such as immunity to noise and process parameter spread, ease and flexibility in design, and programmability, DSP steadily replaced most of the signal processing, which had been traditionally done in analog fashion. Processing the signals digitally has become so successful that the name "digital" has become a marketing icon, and has led consumers to think that if a product is digital it has to be very good.

Even though most of the mainstream signal processing has shifted into the digital domain, there are still some applications for which the ASP is unavoidable. As a matter of fact, the signals and quantities that exist in nature are analog in essence. To interface the inherently analog world, analog circuits such as interface units and data

converters are always required. ASP is also preferred for low-power applications, and to process high-frequency signals, such as radio-frequency (RF) signals. Furthermore, every modern electronic device uses some sort of a power management unit, which is also an analog circuit.

The success of digital design certainly increased the functionality and performance of electronic products. This increase in functionally and performance became a driver for analog design by providing new applications and challenges in the analog domain, as the ASP has to be as high performance as the DSP. For example, the sound information processed by a high-performance digital-signal-processor in a receiver cannot be appreciated, if the digital-to-analog (D/A) converter and the power amplifier does not reproduce a high-fidelity analog signal from the "1"s and "0"s generated by the DSP. Further, the complexity of modern digital design requires very elaborate power management units, which also fuel the analog circuit design and research in this field. Thus, as pronounced by many experts, analog circuit design will continue to prosper thanks to digital design.

Data converters link the digital domain with the analog signals of the real world with the aid of sensors and transducers. While signal acquisition is performed by analog-to-digital converters (ADCs), signal transmission to the real world is facilitated by DACs. To exploit all the processing power and possibilities provided by the DSP, the signals have to be faithfully acquired from, and transmitted to the real world. For faithful signal acquisition, processing, and transmission, each unit in a signal-processing chain has to be at least as accurate as the whole system. However, typically, ADCs limit the overall accuracy in a signal-processing chain. Therefore, improving

the performance of the ADCs is vital to improve the performance of modern signal-processing systems.

The types of data-converter systems can be simply categorized in two major groups as Nyquist-rate and over-sampling converters. These categories are common to both ADCs and DACs. For the sake of simplicity, only over-sampling and Nyquist-rate ADCs are explained in the following.

The frequency of the clock signal used in over-sampling ADCs is very high compared to the bandwidth of the processed signal. Over-sampling ADCs not only exploit the in-band noise reduction resulting from over-sampling but also reduce the in-band noise by noise shaping and filtering the out-of-band noise. Since the spectrum of the processed signal covers only a small fraction of the Nyquist bandwidth, the shaped noise can be filtered outside the signal bandwidth in the digital domain. As a result, over sampling, and noise shaping and filtering can result in exceptional accuracies. This is true especially for over-sampling converters used in sensor interfaces and audio systems, whose accuracies can extend to 24 bits. However, because of the necessity to over-sample, the bandwidth and frequency of the signals that can be processed by oversampling converters are limited. Because this research concentrates on Nyquist-rate ADCs the over-sampling converters will not be discussed any further.

Nyquist-rate ADCs use clock frequencies, which are not very high compared to the frequency of the processed signal. Nyquist-rate ADCs are used to digitize high-frequency and/or high-bandwidth signals. Therefore, most of the time, oversampling is not practical. Thus, although sampling the signals at a high rate has well-known advantages, these advantages are not explicitly exploited by Nyquist-rate ADCs. Even

though, Nyquist-rate ADCs can digitize signals at very high speeds, their accuracy is typically limited to about 14 to 16 bits. Further, sometimes the frequency and bandwidth of the processed signal cannot be predicted in advance as in the case of instrumentation applications. Under these circumstances, the use of Nyquist-rate converters can be the only choice. Nyquist-rate ADCs also have small input-to-output latency, which can be very important in control applications.

Nyquist-rate analog-to-digital (A/D) conversion can be done in several different ways, which may involve a binary or systematic search. Similar methods can be used in digital-to-analog (D/A) conversion. However, some techniques are less meaningful in D/A conversion. For example, binary-search technique is not very meaningful in D/A conversion; however, almost all Nyquist-rate DACs are flash in nature. The flash D/A conversion technique requires an arithmetic summation of a set of weighted quantities. In contrast, almost all A/D conversion algorithms can be realized in various ways. This variety is simply a result of finding effective solutions to a difficult design problem and indicates the inherent challenge in ADC design. The differences in the design challenges of ADCs and DACs are also reflected by the performance of the state-of-the-art designs found in the literature. Although, a 1 GHz, 10-bit DAC is state of the art in DAC design, only an 8-bit, 800 MHz converter represents the state of the art in ADC design. The mentioned designs were designed in CMOS processes.

The performance deficiency seen in ADCs is a result of the nature of the input they process. Because of the continuous nature of the analog signals they digitize, ADCs suffer several problems such as signal and clock skew, clock jitter, nonlinear input impedance, number of components, chip size, power dissipation, etc. The severity

of these problems is somewhat related to the ADC architecture and sometimes limits the practicality of certain architectures. For example, the accuracy of flash converters is accepted to be limited to about 8 bits. This limit is caused by the extreme parallelism incorporated in the architecture, which results in unacceptable chip size and power dissipation for resolutions beyond 8 bits. The chip size further aggravates the problems associated with signal and clock routing in flash converters. Although the flash architecture yields the fastest converter in a given process, because of the problems mentioned above, different architectures can be chosen to trade resolution with speed.

If two-step or subranging architectures are used instead of the flash architecture, the number of comparators required for the conversion can be reduced significantly. However, two-step or subranging architectures achieve rather smaller conversion rates. The folding technique is another attempt to reduce the chip size and component count for a desired resolution. The pipelined architecture is a more specialized application of the two-step architecture, which results in low-power, small, and high-accuracy converters. Nonetheless, pipelining requires precise and repetitive ASP between the stages, which is typically performed by high-gain operational transconductance amplifiers (OTAs) [1,2]. In modern sub-micron processes, the necessity of precise ASP typically limits the conversion speed of pipelined ADCs to a few hundreds of MHz. The pipelined architecture can be further specialized and pipelining can be done in time rather than in space. Pipelining in time results in the successive-approximation architecture (commonly, successive-approximation technique is denoted by SAR, which

stands for successive-approximation register). The converters using the SAR architecture can be very low power, compact, and high resolution. However, the conversion speed of SAR ADCs is typically limited to a few tens of MHz. Besides, the pipelining technique can be applied to two-stage architectures, thereby the number of stages can be further increased without reducing the conversion speed. The resulting architecture is commonly referred to as a multi-bit-per-stage pipelined ADC.

All non-flash ADCs require some sort of a sample-and-hold function for consequent conversion operations. Further, a high-performance sample-and-hold amplifier (SHA) can significantly improve the dynamic performance of high-speed ADCs. For example, a front-end SHA can alleviate some of the problems associated with chip size, and clock and signal skews. The stages following the SHA, can enjoy sampled signals, which relax clock and signal skew, and jitter problems. Thus, even a flash converter can benefit from a good front-end SHA. Besides, a front-end SHA can ease the design challenges associated with frequency multiplication and its undesirable effects in folding ADCs. In fact, this is a very good example that demonstrates the impact of a high-quality front-end SHA on the dynamic performance of the A/D conversion.

The types of SHAs used in an ADC differ depending on the process used in the design [3]. Switched-buffer SHAs are used in bipolar processes, including bipolar complementary metal oxide semiconductor (BiCMOS) processes. In extreme cases, diode-bridge samplers are used in exotic processes where Schottky diodes are available. The diode-bridge technique results in the fastest SHAs because the Schottky diodes, which don't suffer minority carrier storage, can be switched at very high frequencies

[4]. Since voltage sampling is not inherent in bipolar junction transistors (BJTs), the SHAs designed in bipolar processes typically use some sort of current switching to sample and store the input signal.

On the other hand, voltage sampling is inherent in CMOS processes. Therefore, a single metal-oxide-semiconductor field-effect transistor (MOSFET) and a capacitor can function as an SHA. This SHA scheme is known as passive CMOS SHA. This architecture has well-known problems such as clock feed-through, charge injection, and nonlinear on-resistance. To solve these problems, several techniques have been developed such as clock boosting and bootstrapping. Further, high-gain OTAs can be used to assist the sampling operation, which results in active CMOS SHAs. The accuracy of the active CMOS SHAs can be superior to their passive counterparts; nonetheless the speed of active CMOS SHAs is limited by the gain-bandwidth product of the OTAs incorporated in their design. The accuracy of the passive CMOS SHAs is limited to about 8 bits. The spurious-free dynamic range (SFDR) of the passive CMOS SHAs is notoriously difficult to predict beyond 8-bit accuracy. However, they can attain very-high sampling rates. More predictable performance and higher accuracies can be achieved with switched-buffer SHAs at high-sampling frequencies. As mentioned earlier, the switched-buffer technique is a sampling method, which is more suited for bipolar process technology [5]. However, the same principle can be applied in CMOS processes [6]. Switched-buffer SHAs use local feedback; thus, their sampling rate is not as significantly limited as their CMOS counterparts.

Nonetheless, the design of switched-buffer SHAs in CMOS processes has its own problems because of the inferior performance of the MOSFETs, and the bipolar

switched-buffer SHAs are superior to their CMOS counterparts. For instance, the state of the art in switched-buffer design in CMOS is represented by a 10-bit 185 MSample/s SHA, which is far less impressive than a 10-bit, 1 GSample/s bipolar design.

In conclusion, it is clear that CMOS technology is the dominant process technology in today's semiconductor industry - thanks to the revolution of the digital CMOS design. Further, the most critical unit in a signal-processing chain is the ADC. Therefore, this research focused on developing ways to design a high-speed ADC at medium resolution with the use of a two-step architecture in a CMOS process. The design leveraged open-loop architectures and current-mode circuits to achieve high conversion speed. A high-speed switched-buffer SHA architecture was proposed which best suited for the desired characteristics. The design and characterization of the SHA and ADC chips were the main focus of this research. However, other circuits used in A/D conversion, such as programmable-gain amplifiers and pre-charge buffers were also studied.

CHAPTER II

OVERVIEW OF NYQUIST-RATE ANALOG-TO-DIGITAL CONVERTERS

The popular topologies preferred to design high-speed, medium-resolution ADCs are flash, two-step (subranging), folding, pipelined, and interleaved architectures. The speed in A/D conversion is achieved by parallelism in the architecture, which is fully exploited by the full-flash architectures. The price paid for the superiority in conversion rate is an exponential increase in area and power consumption with increasing resolution. The excessive increase in area and power consumption also aggravate other design issues such as matching, self-heating, input capacitance (thus bandwidth), and clock and signal distribution.

Limitations of a particular ADC structure can be compensated by combining several techniques. Thus, it is not surprising to encounter ADCs utilizing pipelining, folding, and averaging techniques simultaneously [7–16]. Popular Nyquist-rate ADC architectures are discussed briefly in the rest of this chapter. The pros and cons of these architectures are also highlighted.

2.1 Flash Analog-to-Digital Converters

The flash topologies fully exploit parallelism as the conversion is done at once with single sampling. That is why flash converters are commonly called parallel converters. The flash architecture yields the fastest conversion speed in a given process technology

[1, 14–18]. The block diagram of an N bit full-flash ADC is given in Figure 1. The operation of the architecture can be summarized as follows. The reference voltage, V_{Ref}, is divided into 2^N levels by a resistor string, Figure 1. Each tap of the resistor string generates a comparison level for a comparator. These comparison levels and comparators make up a comparator bank by which the analog input can be compared to the reference voltage with $V_{Ref}/2^N$ accuracy. After a comparison phase, while the comparators whose comparison level is smaller than the analog input produce a low logic level at their output, the rest produce a high logic level. The outputs of the comparators generate a string of highs, which carries the amplitude information of the input signal. This string is commonly referred to as thermometric code. This code is then converted to the desired digital code (typically to gray then to binary code) by a decoder [1, 2].

Perhaps the only advantage of the full-flash architecture is the high conversion speed, since all the other design parameters such as power and area are sacrificed in favor of speed. The number of components (resistors, comparators, preamps, etc.) increases exponentially with resolution in the full-flash architectures. On the other hand, the difference between two consecutive levels, which corresponds to one least significant bit (LSB), decreases exponentially as the resolution of the converter increases. This contradiction puts stringent limits on the comparator offset and the matching between a large number of resistors, especially if the resolution of the converter is high. Besides, as the resolution increases, settling of the signal at the resistive ladder taps and loading of the resistive string become major problems in terms of

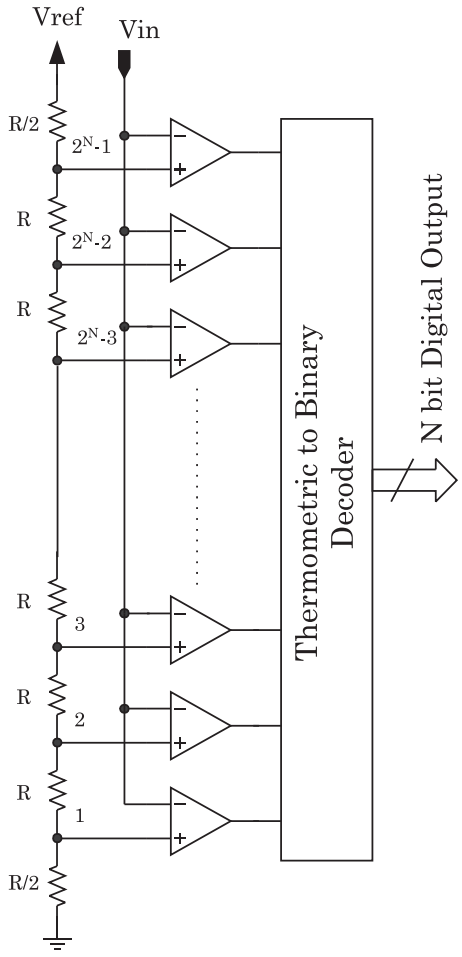


Figure 1: Block diagram of an N bit flash ADC.

power consumption and area (or matching). Since the input is compared with different levels by $2^N - 1$ comparators simultaneously, the analog input experiences a huge capacitive load, which is nonlinear. This high capacitive loading severely affects the speed and increases the power consumption and degrades the linearity of the input buffer. Furthermore, kick-back from the comparators can cause significant errors because of the simultaneous comparison performed by a large number of comparators. In addition, in applications where a front-end SHA is not preferred, signal and clock skew becomes a critical problem. These problems are mainly caused by the large

area occupied by the converter, which forces the clock and input signal to travel long distances. On the other hand, routing a signal over a long distance introduces delay. The unequal delay experienced by the clock and signal through reaching a particular comparator gives rise to errors.

The disadvantages of this technique are listed below [1, 2]:

- Necessity of good matching between a large number of integrated resistors and comparators
- Sensitivity to comparator offset
- Loading of the resistor ladder and settling time of the tap voltages
- Large and nonlinear input capacitive load
- Inherent limitation to the maximum achievable resolution due to large chip area and power consumption, which is a result of the brute force approach followed in this architecture (i.e. full parallelism in the structure, to have an N bit ADC 2^N resistors and $2^N - 1$ comparators are required).

Even though a reported 10-bit full-flash ADC exists, [19], the achievable resolution with this architecture is believed to be limited to 8 bits. Nonetheless, under extreme consumer demand, the industry offers 10-bit full-flash ADCs.

2.2 Two-Step Analog-to-Digital Converters

To relax the system requirements of a flash converter (i.e. to reduce area, power consumption, capacitive loading, and increase maximum achievable accuracy) two-step (subranging) technique can be exploited at the expense of conversion speed,

[1,2,20]. The block diagram of a two-step ADC is depicted in Figure 2. A conversion cycle can be explained as follows: First, the front-end SHA samples the input. Then, a low-resolution ADC quantizes the sampled input signal. Since the resolution of this stage is lower than the total ADC, this step is referred to as coarse quantization. From the output word of this ADC, an analog signal is generated by a DAC. The analog signal at the output of the DAC is then subtracted from the sampled input to generate the residue signal, which is then amplified by an amplifier. This residue is quantized by a second low-resolution ADC. Because of the amplification of the residue, the second low-resolution ADC, in fact, quantizes the residue in finer steps. Therefore, this step is referred to as fine quantization. The outputs of the fine and coarse ADCs are appended to generate the total digital signal representing the amplitude of the input. The A/D conversion is done in two steps, coarse quantization followed by fine quantization, hence the name.

An auxiliary SHA may be used to hold the input signal for subtraction, amplification and fine quantization phases, Figure 2(b). Thereby, the coarse and fine quantization steps can be pipelined. While the D/A conversion, subtraction, and fine quantization are done, the front-end SHA and coarse ADC can deal with another sample of the input. The SHA_2 function is typically incorporated in the M-bit ADC in switched-capacitor implementations. Furthermore, with the possibility of error correction, the accuracy requirements of the coarse ADC can be relaxed [2].

Compared to the full-flash technique, the two-step technique gives rise to tremendous savings in comparator and preamplifier count. These savings result in more reasonable power and area consumption allowing high-resolution converter designs.

For example, to design an 8-bit two-step ADC, which has 4-bit coarse and fine quantization stages, 30 comparators are required, as calculated by (1).

$$(2^4 - 1) + (2^4 - 1) = 30 \tag{1}$$

For the same number of bits, the number of comparators required for the full-flash architecture is 255. This simple example demonstrates an important trade-off in the brute force approach followed in the full-flash architectures.

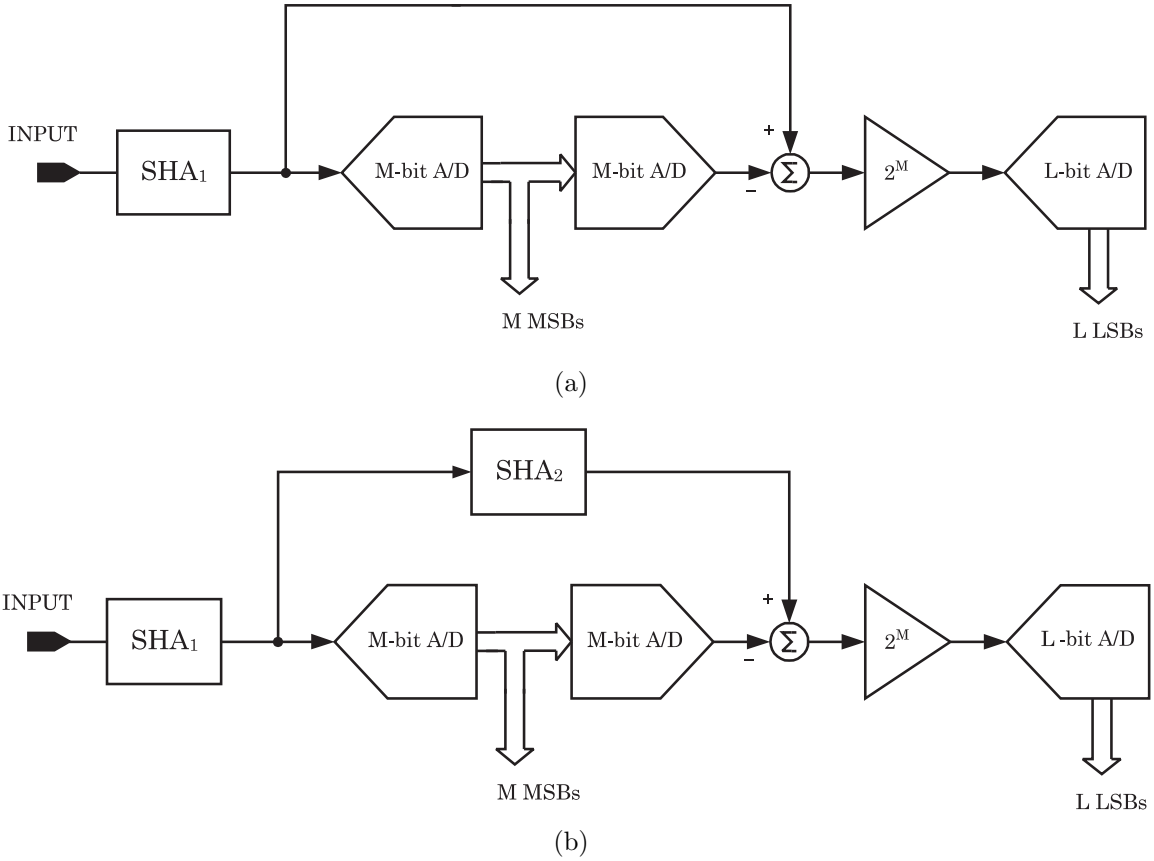


Figure 2: Two-step ADC. (a) Without pipelining. (b) With pipelining.

The main limitations of the two-step topology are

- Necessity of a high-performance front-end SHA,
- Necessity of highly accurate and fast amplifier, and subtractor,
- Necessity of an amplifier with full swing capability within the clock period, because of the weak correlation between successive samples [1, 2].

As a conclusion, the two-step architecture trades speed and latency with area, power, and resolution. A good reference for the subranging technique is [20].

2.3 Folding Analog-to-Digital Converters

The time required to generate an analog signal from the outputs of the coarse ADC and the necessity of a somewhat low speed but accurate subtractor limit the speed in two-step converters. If pipelining is not used between coarse and fine quantization steps, the speed is further reduced because of the time required for fine quantization. The folding technique evolves from the desire to generate the residue signal without using an SHA, DAC, and high-accuracy subtractor. A conceptual block diagram of a folding ADC is given in Figure 3. A folding ADC generates the residue by analog preprocessing. This preprocessing can be visualized as wrapping and unwrapping the input signal onto a virtual cylinder, Figure 4. While a coarse quantizer indicates the number of turns of the cylinder, a fine quantizer indicates the position of the signal on the cylinder. The folded (residue) signal generated by a folding ADC is depicted in Figure 5. The generation of the folded signal as it is depicted in Figure 5 is quite ideal. During analog preprocessing, it is very difficult to generate highly

linear folded signals. Since the high-frequency components are suppressed because of limited bandwidth, especially the "tips" of the folded signal are rounded. However, even though the tips are rounded, the difference -in this case the error- between the ideal and practical folded signal reduces to zero at the zero crossings. Therefore, the amplitude of the signal can be determined accurately at the zero crossings of the folded signal, Figure 6.

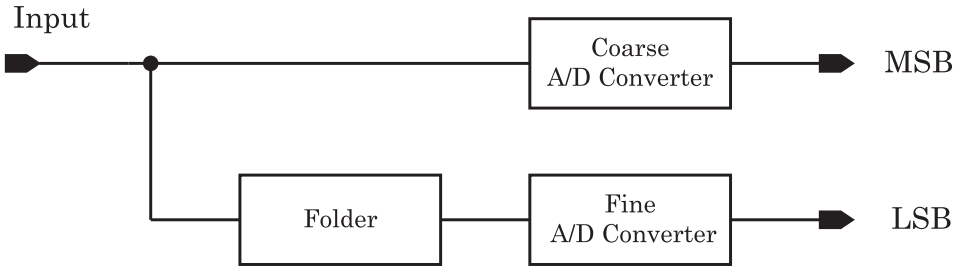


Figure 3: Conceptual block diagram of a folding ADC.

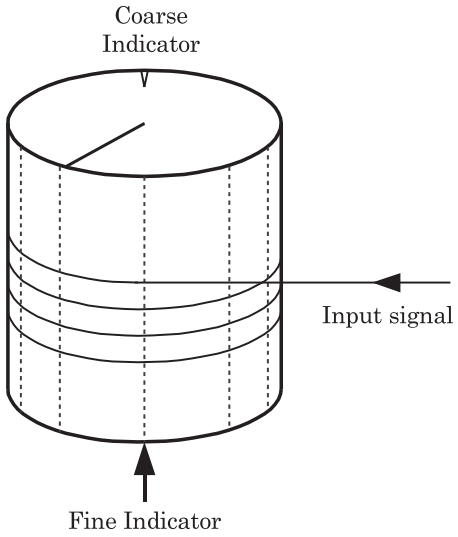


Figure 4: Illustration of the folding technique.

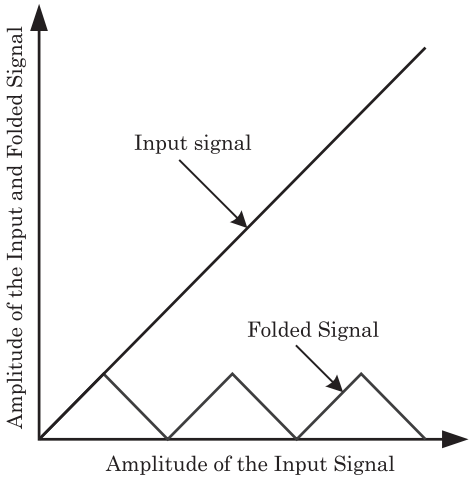


Figure 5: Input signal versus the unfolded and folded output signals.

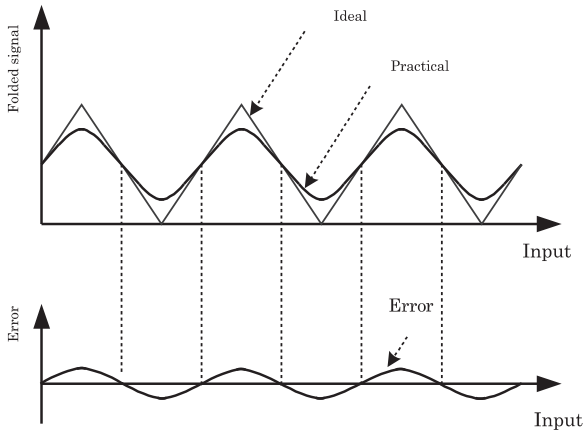


Figure 6: The residue generated by an ideal folder, realistic folder and the difference between the two signals.

One important limitation of the folding technique is the necessity of a much higher bandwidth than that of the processed signal. When the input signal swings full scale experiencing a single zero crossing, the folded signal crosses zero as many times as the folding factor. This translates to a frequency multiplication by the folding factor. In practice, the folding factor is generally limited to about eight to avoid excessive frequency multiplication, [12, 13].

To depend solely on folding to digitize the input may require unattainable bandwidth requirements, undesirable high power and area consumption, and high noise levels even for medium resolutions. Instead, interpolation is used to increase the number of zero crossings [12–14, 16, 18, 21–23]. The main idea of interpolation starts with the generation of additional zero crossings by incorporating "phase quadrature" folded signals. These signals are summed with proper weights to generate the desired additional zero crossings as illustrated in Figure 7. Cascading is another technique to further increase the resolution without having area, power and noise penalties [8, 12, 13]. In addition to these, most of the time a front-end SHA amplifier is used to relax the problems encountered as a result of limited bandwidth and frequency multiplication. The SHA also provides the possibility of pipelining [8–13]. The main limitations of the folding technique are matching between the folding amplifiers and interpolating resistors and frequency multiplication. However, the matching problem can be relaxed with resistive or capacitive averaging, and a front-end SHA can alleviate the frequency multiplication. A popular realization of a folding amplifier is the cross-coupled differential-pair bank, which is depicted in Figure 8. Folded signals as well as the phase-shifted signals are easily generated with this topology.

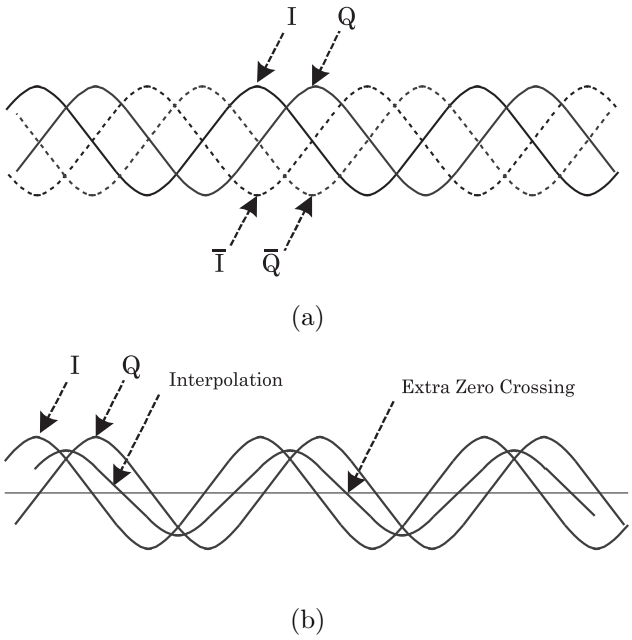


Figure 7: Interpolation (a) Quadrature signals generated from the same input. (b) Generation of an additional zero crossing by interpolation.

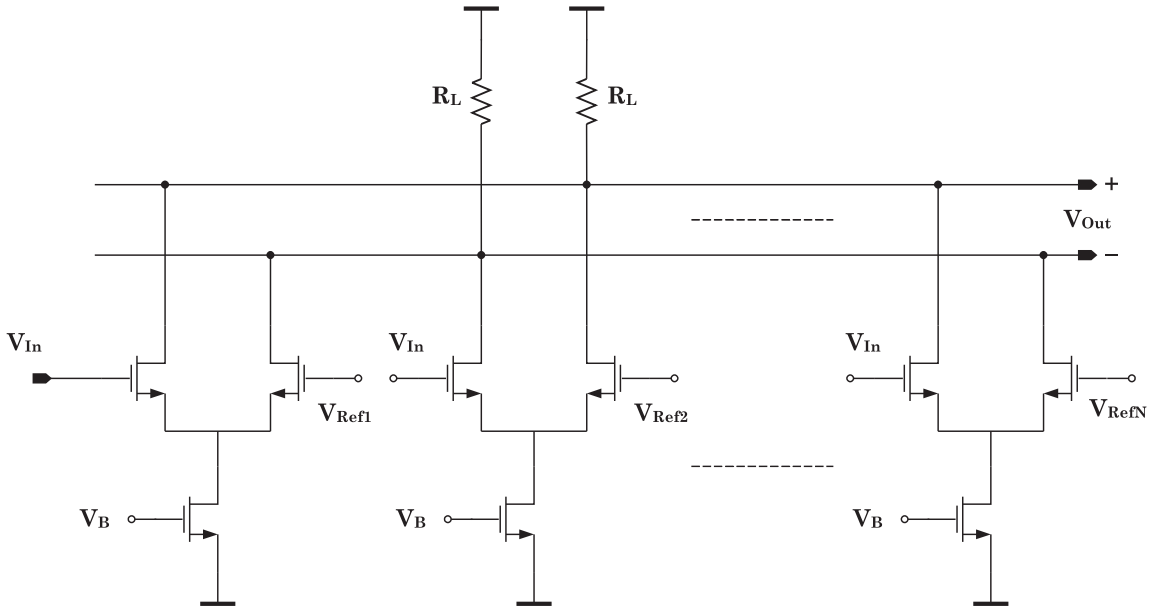


Figure 8: A popular folding amplifier topology.

2.4 Pipelined Analog-to-Digital Converters

Although it is often exploited in two-step and folding ADC designs, pipelining is the more generalized application of the two-step technique utilizing multi-stage cascade

of low-resolution stages. The conversion speed is determined by the speed of a single stage, which is almost always the first stage. Since overall conversion speed is determined by a single stage, the attainable conversion speed can be quite high. On the other hand, repetitive precise ASP necessitates stringent specs for gain errors of the SHA and interstage amplifiers. A block diagram of a multi-stage pipelined ADC is provided in Figure 9.

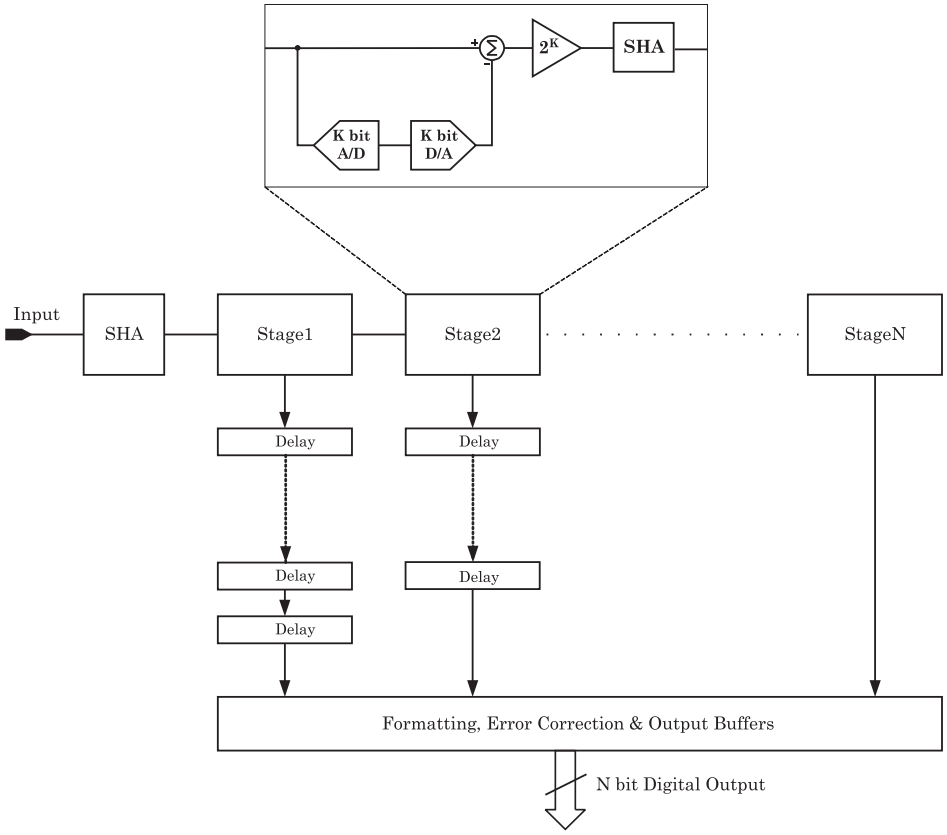


Figure 9: Block diagram of a pipelined ADC.

The main advantages of the multi-stage pipelining technique over the two-step technique are the necessity of less complex and lower resolution ADC and DAC sub-block, and smaller interstage gain. The reduced complexity is often exploited by combining several functions in a single circuitry. For example, the DAC, subtractor,

and SHA can be implemented by a single switched-capacitor circuit in CMOS and BiCMOS technologies. This circuitry is commonly referred to as the multiplying DAC, MDAC.

The accuracy required from the stages reduces as the signal propagates down stream. For example, for a two-bit-per-stage implementation of an N-bit pipelined ADC, the sub-ADC consisting of all but the first stage can be treated as an $(N-2)$-bit ADC, relaxing the accuracy requirements of the first stage of this $(N-2)$-bit ADC by four. Consequently, the accuracy of each stage can be relaxed by four compared to the previous stage. This relaxation can be exploited to reduce the power and area consumption. Another important issue is the possibility of digital error correction [24–33]. With error correction, the accuracy of the ADCs in each stage can be as accurate as the resolution of the stage itself. However, error correction does not relax the accuracy requirements of the DACs used in the stages. Moreover, the 1.5-bit-per-stage architecture has been the most popular multi-stage pipeline ADC architecture with digital error correction, [24–26].

2.5 Successive-Approximation Analog-to-Digital Converters

A true binary search algorithm is implemented in the SAR topology. A SAR ADC consists of a front-end SHA, a comparator, a DAC, and a successive-approximation register as shown in Figure 10. The front-end SHA samples the input and holds while the binary search is performed. First, the successive-approximation register produces a half-scale digital word, which is all LOWs except the most significant bit (MSB),

that is, 100...000. The DAC generates a half-scale analog signal with this digital word. The input is compared with this half-scale analog signal. If the input is larger than the half-scale analog signal, the MSB is set to HIGH, otherwise, the MSB is set to LOW. With the first approximation attempt, the MSB is decided. In the second approximation the second most significant bit is set to HIGH. If the MSB is set to HIGH in the first approximation, this digital word results in an analog signal, which corresponds to 3/4 of the full scale. However, if the MSB is set to LOW, this results in an analog signal, which corresponds to 1/4 of the full scale. The input is once again compared to the analog signal generated by the DAC and the second most significant bit is decided. The bits constituting the digital output are generated sequentially one at time after each approximation attempt starting with the MSB. Figure 11 illustrates the successive approximation. The whole conversion lasts as many clock cycles as the number of bits in the digital output. Thus, the conversion speed is quite lower than the previously mentioned architectures. A popular switched-capacitor implementation of the SAR topology, which is based on charge redistribution, is given in Figure 12. In fact, this topology has been the last major architectural innovation in A/D conversion [34].

The SAR architecture yields very compact and power efficient ADCs, with medium-to-high resolutions. As a result of these properties, SAR converters are preferred in portable applications where high resolution is required at low conversion rates.

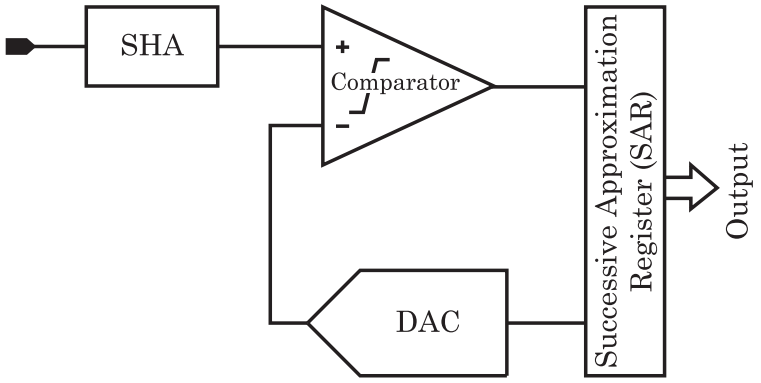


Figure 10: Block diagram of SAR architecture.

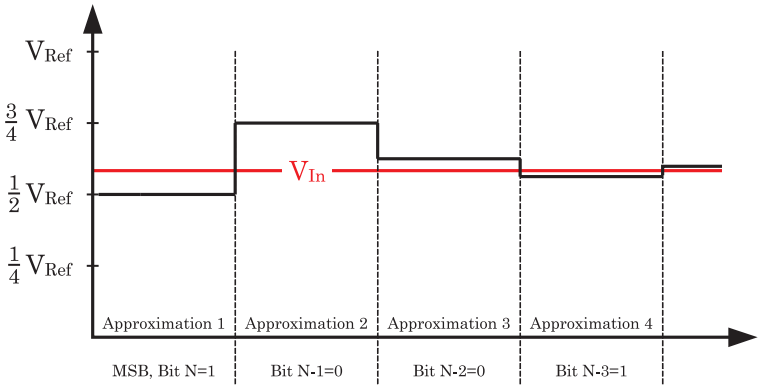


Figure 11: Illustration of successive approximation. The bits constituting the digital output is generated one at a time after each approximation attempt starting with the MSB.

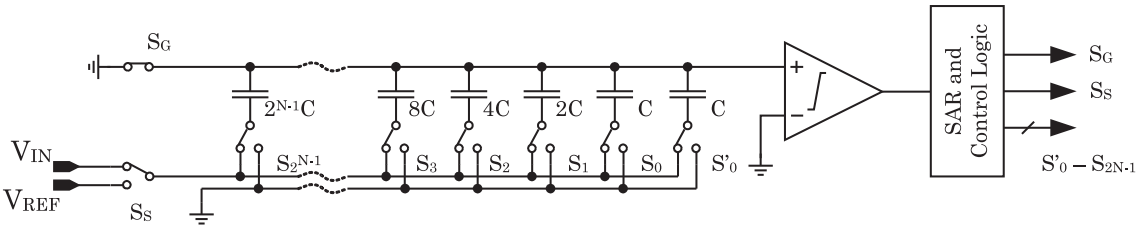


Figure 12: A popular implementation of the SAR ADC based on charge redistribution.

2.6 Interleaved Analog-to-Digital Converters

Interleaved ADCs simply exploit the fact that high conversion speed in A/D conversion is achieved by parallelism in the architecture. For an interleaved structure of N

ADCs, the throughput of the overall converter is N times that of the single one. A generic block diagram of an interleaved ADC is shown in Figure 13. Thus, ideally the speed, power, and area requirements of each ADC can be relaxed. However, other complications typically prevent these relaxations. The interleaved structure suffers several problems, which are listed below.

- The structure incorporates entire ADCs,
- The Matching requirement between the ADCs comprising the system is quite stringent,
- The gain error causes amplitude modulation of the signal,
- The timing error causes phase modulation of the signal,
- Offset mismatch gives rise to spurs in the band of interest; therefore, degrades SFDR, [1, 2].

Because of these severe limitations offset and gain calibration techniques have to be employed to achieve an acceptable performance [1, 2, 35].

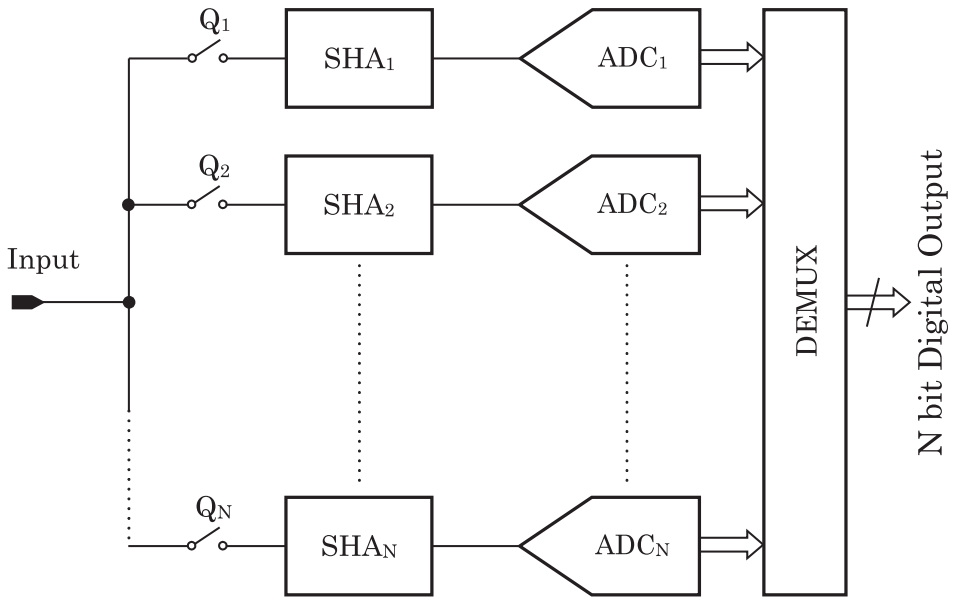


Figure 13: Conceptual block diagram of an interleaved ADC.

Nyquist-rate ADC topologies are discussed above. Each converter topology has at least one parameter that can be optimized to the desired value more easily than others. The flash topology results in the fastest converter in a given process. On the contrary, the successive-approximation topology results in the lowest power dissipation. For an easy comparison, several properties of the Nyquist-rate ADC topologies are tabulated in Table 1.

Table 1: Performance Comparison of Nyquist-Rate ADCs

Converter Topology	**Resolution**	**Conversion Rate**	**Power Dissipation**
Flash	Low	Very High	Very High
Folding	Medium	(Very) High	High
Two-Step	Medium-High	High	High
Pipelined	Medium-High	Medium	Medium
SAR	High	Low	Low
Interleaved	Low	Very High	Very High

CHAPTER III

ANALOG-TO-DIGITAL CONVERTER DESIGN TRENDS

The flash, folding, and two-step (more generally, multi-bit-per-stage pipelined ADC) architectures result in high conversion rates. As discussed earlier, even though the flash converter results in the fastest converter in a given process, it has limited resolution, which is accepted to be 8 bits. The folding technique results in rather slower conversion rates. However, it is more area and power efficient. Thus, the attainable resolution with the folding technique can be as high as 10-12 bits. Cascading and pipelining techniques can also be exploited to achieve higher resolutions with the folding technique. In principle, a folding ADC, which uses pipelining is a multi-bit-per-stage pipelined ADC. Pipelined multi-bit-per-stage ADCs can operate at high conversion rates with 10-, 16-bit resolutions. The most critical block in this architecture is the front-end SHA, which enables pipelining or two-step operation in the most basic structure. Since multi-bit-per-stage ADCs have quite modular architectures, their improvement toward higher speed or resolution is relatively easy. Because of this versatile modularity property, the multi-bit-per-stage architecture is chosen in this research.

Over 200 papers published in journals and conferences were reviewed to provide a general idea about the main trend in ADC design, applications, and architectures. Performances of the prototype chips are tabulated in the appendix. The famous

Walden's chart is reconstructed with this data to be able to see the main trend in resolution versus conversion rate. Walden's survey is recently updated by Boris Murmann [36, 37]. The improvement in resolution and conversion rate is sporadic. The main trend continues to be design for mobile consumer applications. Because of the market-driven nature of the problem, there is no architectural improvement. Rather, the faster submicron processes and their nonstandard features are exploited to improve power and sometimes resolution for a given conversion rate, which is often below 50 MHz [24–26, 28, 30–32, 38].

Low conversion rates allow the usage of switched-capacitor circuits. Thus, most of the implementations use the classical pipelined architecture, which consists of multi-stage cascade of low-resolution stages. Furthermore, in recent years significant improvement has been accomplished in error correction, which has allowed the design of pipelined ADCs with 14-16 bit accuracies. However, the correction schemes are rather complex and require significant design overhead [27, 33, 39–42]. Another less attractive target has been GHz-range conversion speeds. In this range, full-flash and folding architectures are preferred for 6- and 8-bit accuracies, respectively. Most of the time, averaging and interpolation are used to improve matching, reduce input impedance, and save power and area. These ADCs find their place in radar, imaging, satellite-communications, and instrumentation applications. Yet, another drive for high-speed, high-resolution ADCs is communication infrastructure applications, which require about 14 bits of resolution with $100 - 200$ MHz sampling rate. For communication infrastructure applications, the preferred ADC architecture is multi-bit-per-stage pipelined converters with 3- to 6-bit stage resolutions.

The reconstructed Walden chart is given in Figure 14. Clock jitter barriers of 1, 0.5, and 0.3 ps are provided for easy comparison. Today's state of the art probably, corresponds to an ideal converter which has 0.5 ps jitter. A more comprehensive survey on ADC performance is reported by Boris Murmann, [36, 37].

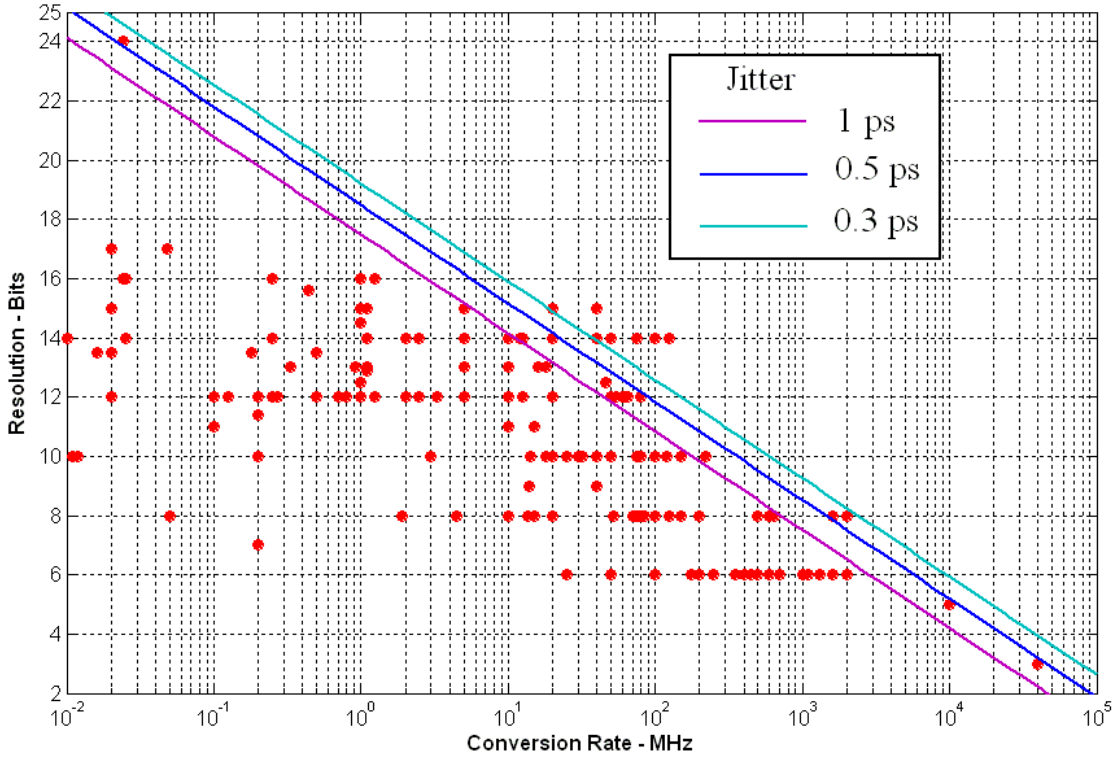


Figure 14: Walden chart generated from data given in the appendix.

3.1 Preferred Sample-and-Hold Amplifier Architectures in Nyquist-Rate Analog-to-Digital Conversion

The front-end SHA in a high-performance ADC system suffers the most demanding dynamic requirements. After the front-end SHA, the signal is sampled (discretized in time). As a result, the stage following the front-end SHA can have less demanding dynamic performances. For example, clock jitter is not a significant problem for the stages that process discretized signals.

Industrial products and prototype ICs reported in the literature follow four different design strategies to achieve high-performance A/D conversion. These four strategies target different system specifications such as resolution, conversion rate, power consumption, and silicon area. These four A/D conversion strategies and preferred types of SHAs for different architectures are discussed in the following.

The first design strategy is to use the full-flash topology to achieve very high conversion rates [1, 2, 14–19]. Because of the total parallelism exploited in this architecture, the front-end SHA can be avoided and sampling can be done in a parallel fashion with the bank of comparators comprising the topology. However, employing a front-end SHA relaxes problems associated with clock and signal skew. As discussed previously, the exhaustive parallelism in the full-flash topology limits its resolution to about 8 bits because of power and area consumption, clock- and signal-skew problems, and parameter mismatch.

The second strategy is to use the folding architecture, which can also avoid a front-end SHA. However, it has been shown that if the input is discretized, the dynamic performance of a folding ADC improves significantly. Actually, this is one of the

applications in which a discretized signal improves the performance of the overall system. The front-end SHA for a very high-speed, low-resolution folding converter can be a basic CMOS switch, see Figure 15(c). For higher resolutions, a switched-buffer SHA, or at the extreme, a diode-bridge sampler, can be employed. Simplified schematics of a switched-buffer SHA and diode-bridge sampler are given in Figures 15(a) and 15(b).

The two fundamental problems associated with the basic CMOS switch are charge injection and clock feed-through. These problems get worse at high sampling rates, which require switches with high aspect ratios to get satisfactory settling accuracy and linearity. It can be shown that if the hold pedestal can be tolerated, the CMOS switch can be quite linear with a bootstrapped clock. However, this is generally not the case and some kind of pedestal cancelation circuit has to be used. On the other hand, any kind of cancelation circuit deteriorates the distortion and limits the accuracy to about 8 bits. For higher resolutions, the performance of the CMOS switch is notoriously unpredictable.

Switched-buffer SHA topologies have more predictable high-frequency performance. Classical switched-buffer SHA topologies have substantial hold-mode feed-through at frequencies close to the Nyquist rate. Even though it can be extremely fast, the diode-bridge SHA [43] also suffers from hold-mode feed-through as its switched-buffer counterpart. This is an expected result because the switched-buffer SHA has evolved from the diode-bridge sampler [3].

The third strategy is to employ multi-bit-per-stage pipelined or subranging topologies for high-speed and high-resolution applications such as communication infrastructure applications. For this strategy, the best choice is the switched-buffer SHA architecture because of the inherent trade-off between power and accuracy, [20, 44]. Again, the Nyquist-rate operation is problematic with the classical switched-buffer SHAs.

Finally, the last strategy is to use the traditional pipelined ADC architecture consisting of multi-stage cascade of low-resolution stages. These converters are designed for market-driven low-power applications. Because of the demanding interstage ASP, this approach relies on switched-capacitor design. Thus, the SHAs are active CMOS samplers, which require high-gain OTAs, see Figure 15(d). Most of the time the sampling frequencies of pipelined ADCs do not exceed 200 MHz because high-gain OTAs used in these structures operate in closed-loop.

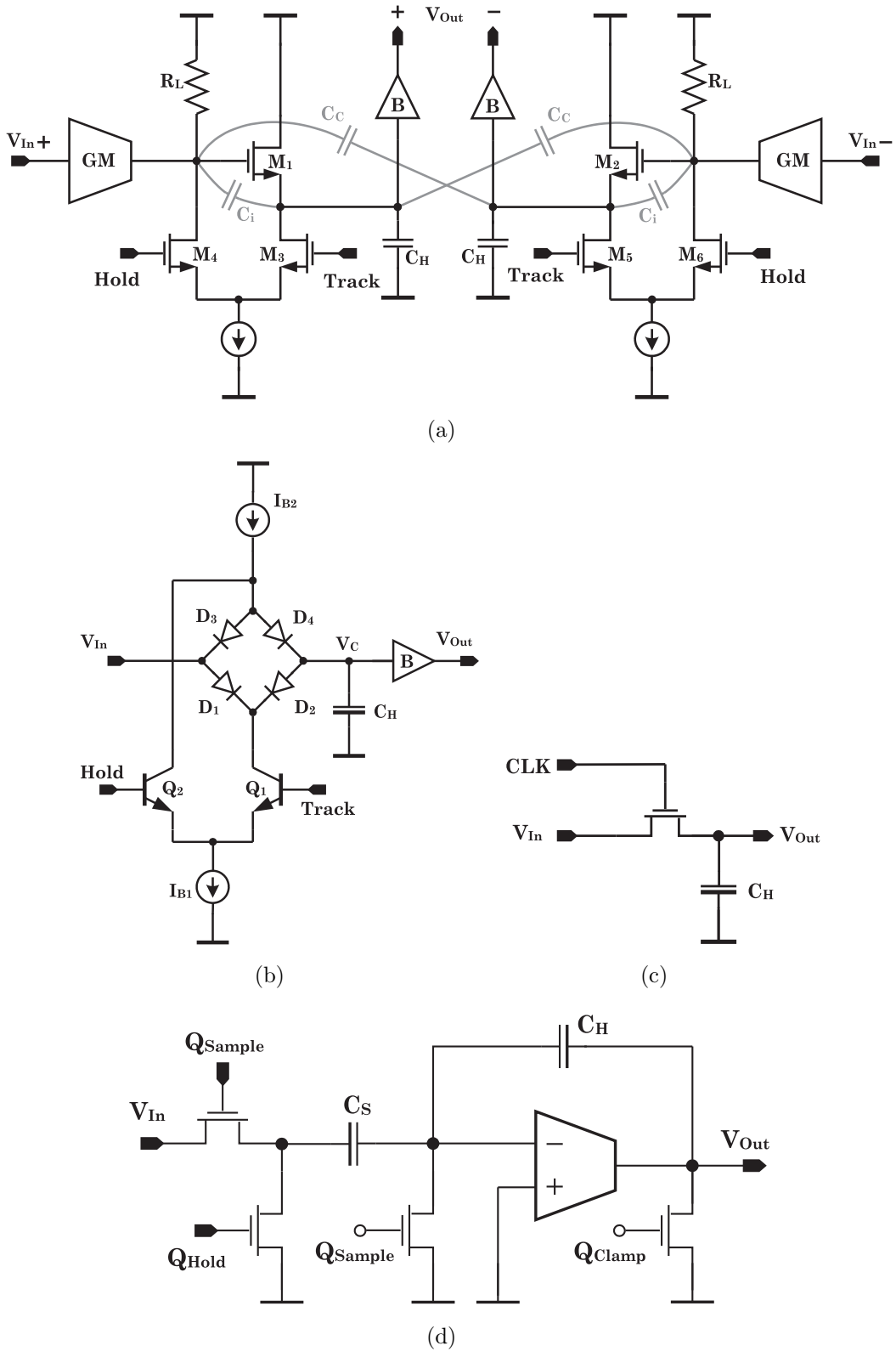


Figure 15: Simplified schematics of SHA architectures. (a) Switched-buffer SHA; differential structure is shown to explain cross coupled capacitor technique. (b) Diode-bride SHA. (c) Passive CMOS SHA. (d) Active CMOS SHA.

CHAPTER IV

DOUBLE-SWITCHING SHA WITH EMPHASIS ON HOLD-MODE ISOLATION

The basic structure of a switched-buffer SHA consists of three parts, which are the input buffer, sampling buffer, and output buffer, Figure 16(a). This architecture has been the classical topology in switched-buffer SHA design [5]. However, the idea is borrowed from the diode bridge SHA whose high-speed performance has been confirmed by several designs [3, 43].

4.1 Limitations of the Classical Switched-Buffer SHA

The main architectural problem with the classical switched-buffer SHA topology is hold-mode feed-through, which becomes worse at frequencies close to the Nyquist rate. This frequency dependent deterioration can be explained as follows. As the frequency of the input signal approaches the Nyquist rate, the signal swing at the input during the hold time approaches the peak-to-peak input signal amplitude. This swing is generally large enough to distort the held voltage because of the inherent coupling capacitor between the input and output of the switching buffer (if the coupling is linear, with a sinusoidal excitation hold-mode feed-through causes gain error rather than distortion). The inherent coupling capacitor, which is represented by C_i in Figure 15(a), is the total device and layout introduced capacitance that couples the input of the switching buffer to hold node during the hold phase. The coupling over

C_i can be attenuated below a certain level by cross-coupled capacitors, which are depicted as C_C in Figure 15(a). However, the attenuation level depends on how well C_C matches C_i. Furthermore, the nonlinearity of C_i reduces the effectiveness of the cross-coupled capacitor technique because of reduced matching and nonlinear signal coupling. There are several interesting examples of this technique in the literature [5, 6, 45, 46].

4.2 Proposed Double-Switching SHA

An alternative to the cross-coupled-capacitor technique can be to switch off the input buffer during the hold phase. This provides a high level of isolation between the input and the held voltage, and enables the aimed performance with input frequencies as high as or higher than the Nyquist rate.

The input buffer can be switched off in two different ways. The first way (previously reported method) is to switch the input buffer from differential-mode (DM) to common-mode (CM) operation, which will be referred to as mode-switching method. The operation of the mode-switching method will be explained with a previously reported topology, whose block diagram is given in Figure 16(b). In this topology, the main OTA of the input buffer (Gm_1) is always on. In the hold phase, a second OTA (Gm_{1ex}) is connected to the output of the input buffer in such a configuration that the differential currents generated by Gm_1 and Gm_{1ex} cancel each other. Note that, in the mode-switching method, the isolation in the hold mode depends on how well the currents generated by Gm_1 and Gm_{1ex} cancel each other. Thus, any mismatch in Gm_1 and Gm_{1ex} deteriorates the hold-mode isolation. Nonetheless, this technique

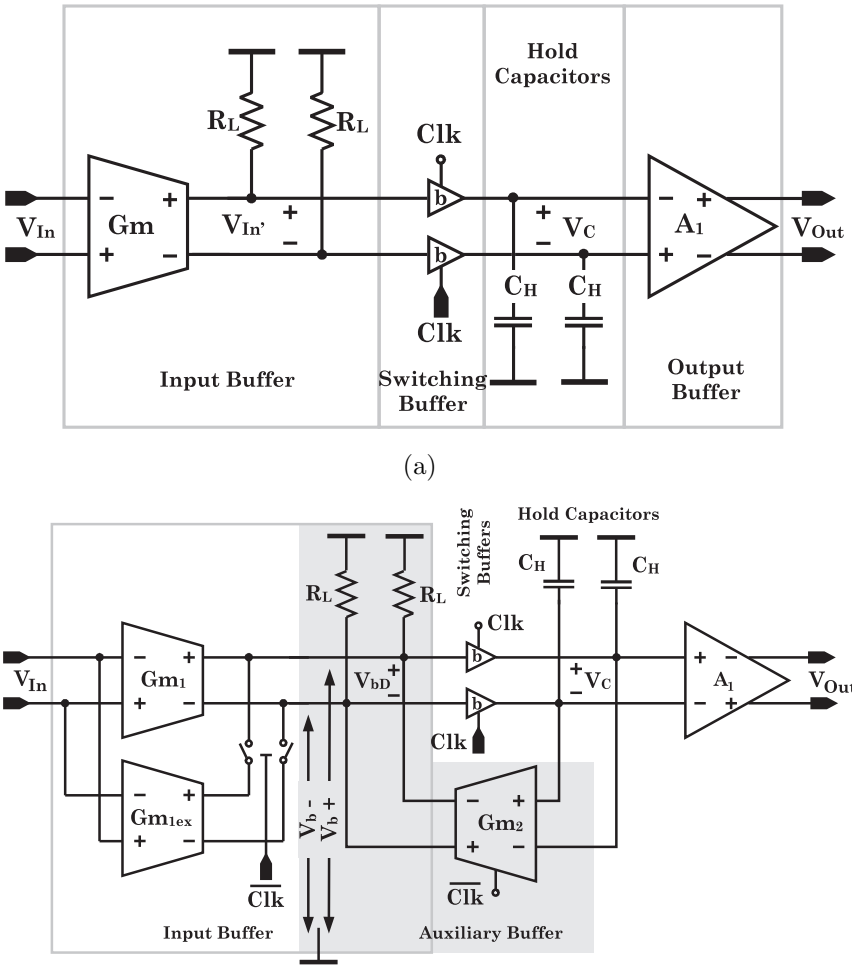


Figure 16: Previously reported switched-buffer SHA architectures. (a) Classical architecture. (b) Mode-switching architecture.

can result in exceptional isolation as demonstrated by [47]. In the track phase, Gm_{1ex} is disconnected from the output of the input buffer. As a result, the input buffer operates in the differential mode.

The proposed (second) method is to switch off the input buffer by steering its output from the actual loads to the dummy loads, [48]. This method will be referred to as output-steering method. A block diagram of the proposed output-steering method is given in Figure 17. The actual and dummy loads are depicted as R_L and R_D

respectively. In the output-steering method, the output current of the input OTA Gm_1 can be switched between its actual $(+, -)$ and dummy $(D+, D-)$ outputs. In this method, the switching is hard. As a result, the output of the input buffer is totally isolated from the input. Because of hard switching, device mismatch is no longer an issue as far as hold-mode isolation is concerned.

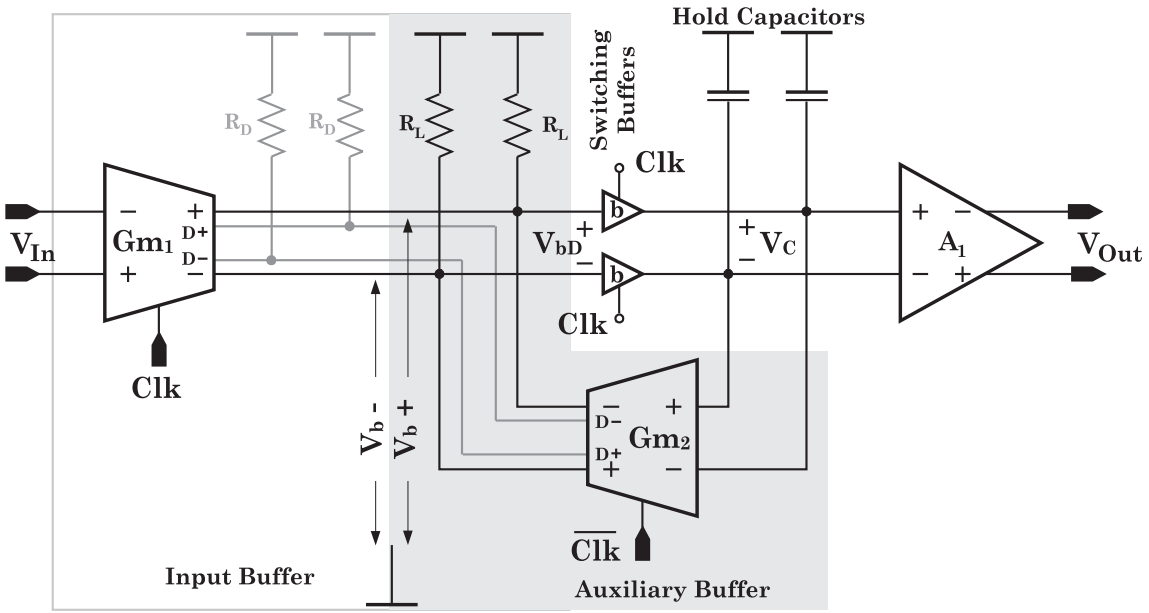


Figure 17: Proposed double-switching switched-buffer SHA.

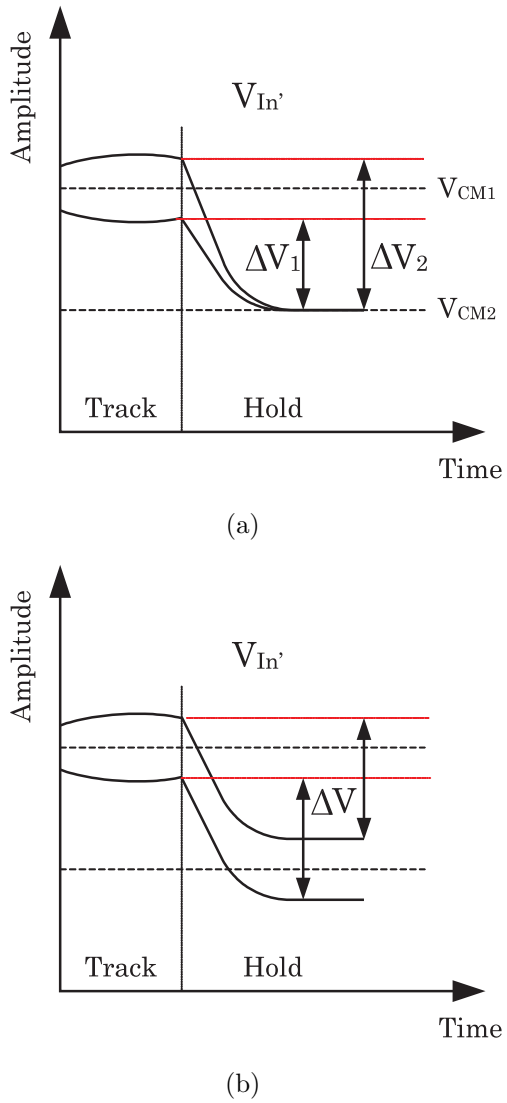


Figure 18: The signal at the input of the switching buffer in double switching SHA topology. (a) Without auxiliary buffer. (b) With auxiliary buffer.

Note that, both of the input-buffer switching architectures employ an auxiliary buffer, see Figure 16(b) and 17. Because, without an auxiliary buffer, both of the input-switching techniques exhibit significant hold pedestal, [47]. The significance of the auxiliary buffer in terms of eliminating the hold pedestal can be explained as follows. To switch the SHA from track mode to hold mode, the CM value of the voltage at the input of the switching buffers is reduced from its track-mode value of

V_{CM1} to its lower hold-mode value of V_{CM2}. Furthermore, the input buffer switches off to improve isolation in the hold mode. Consequently, the differential current running on R_L decays to zero, which means, the differential voltage (V_{bD}) at the input of the switching buffer decays to zero. As a result, the differential branches of V_{bD} (V_b+ and V_b-) experience different jumps while reaching to the lower hold-mode CM level of V_{CM2}. Without an auxiliary buffer, the behavior of V_b+ and V_b- during track- to hold-mode transition is shown in Figure 18(a). The different jumps $\triangle V_1$ and $\triangle V_2$ experienced by V_b+ and V_b- respectively, couple to the hold node (V_C in Figure 16(b) and 17) through any capacitor that couples the input of the switching buffer to the hold node. This coupling, on the other hand, results in hold pedestal. However, the hold pedestal can be reduced significantly if an auxiliary OTA (Gm_2) same as Gm_1 is placed between the hold node and the input of the switching buffer, as shown in Figure 16(b) and 17, [47,48]. In such a configuration, the auxiliary OTA functions as an auxiliary input buffer. Consequently, as the differential current generated by Gm_1 is switched away from the load resistors, a replica of the current generated by Gm_1 is supplied by Gm_2 in the hold mode. Note that, the input of Gm_2 is the held voltage, which is an accurate replica of the input voltage at the end of the track phase. Therefore, V_{bD} is sustained at a value, which ideally corresponds to the differential input signal amplitude at the end of the track mode. With an auxiliary buffer, the behavior of the voltages V_b+ and V_b- during track- to hold-mode transition is shown in Figure 18(b). In this scheme, V_b+ and V_b- experience the same voltage shift $\triangle V$ in reaching the lower hold-mode CM level of V_{CM2}. Consequently, the signal coupling to the hold capacitor is common. As a result, the hold pedestal is substantially lower.

The OTAs - Gm_1 and Gm_2 - are switched to the load resistors alternatively. Note that, when the auxiliary buffer is switched on, the switching buffer is switched off. Therefore, the auxiliary buffer does not operate under positive feedback condition. The skew between the clock signals that switch the auxiliary and the switching buffers can result in positive feedback around the auxiliary and switching buffers. However, clock skew can be minimized by careful layout design and equalizing the load on the clock lines.

The hold pedestal becomes smaller and smaller as the differential currents generated by the two OTAs (Gm_1 and Gm_2) match better and better. Assuming two identical OTAs, this suggests that the gain from the input to the hold node (V_C in Figure 16(b) and 17) should be as close to unity as possible. Furthermore, any phase difference between the input signal and the held voltage increases the hold pedestal [47]. The cross-coupled-capacitor technique can be employed to further suppress any residual pedestal caused by gain and phase mismatch.

The proposed double-switching SHA architecture results in very good hold-mode isolation without cross-coupled capacitors. The proposed double-switching technique shows similarities to the mode-switching technique reported in [47], which uses two input buffers to switch from DM to CM to improve hold-mode isolation. In the mode-switching technique, hold-mode isolation depends on how well the two input buffers match. Since, the proposed output-steering technique uses only one input buffer, it has better hold-mode isolation in the presence of mismatch in the input buffer. Furthermore, in the proposed output-steering technique, the input buffer is implemented with a single OTA, i.e. the transconductance Gm_{1ex} in Figure 16(b)

is not required. As a result, in this design the input buffer is more power and area efficient. The proposed output-steering technique results in about 20-30 % power and significant area savings compared to the mode-switching technique. The details of the transistor level realization of the proposed method are discussed in the following section.

4.3 SHA Circuit Design

The SHA was designed in a single-well 0.18 μm CMOS process. Thick-oxide devices, which can operate with 3.3 V supply voltage, are available in this process. To maximize sampling frequency, only NMOS devices were used as active devices. Further, both thin- and thick-oxide transistors were used to maximize dynamic range. Even though low-threshold-voltage (low V_T) and native transistors were available, such devices were not used in this design. The double-switching SHA is comprised of two main blocks; the input buffer and the switching buffer (the auxiliary buffer is identical to the input buffer), see Figure 17. A simplified schematic of the proposed SHA without an output buffer is provided in Figure 19. The track-mode spurious-free-dynamic-range (SFDR) of both the input buffer and switching-buffer were designed to be 70 dB. Note that, some overhead is necessary to guarantee 10-bit linearity (62 dB THD) in the hold mode because the combined distortion of the input buffer and the switching buffer determine the linearity of the SHA. In the following, the optimization of the input and switching buffers is discussed, and some important design details are highlighted.

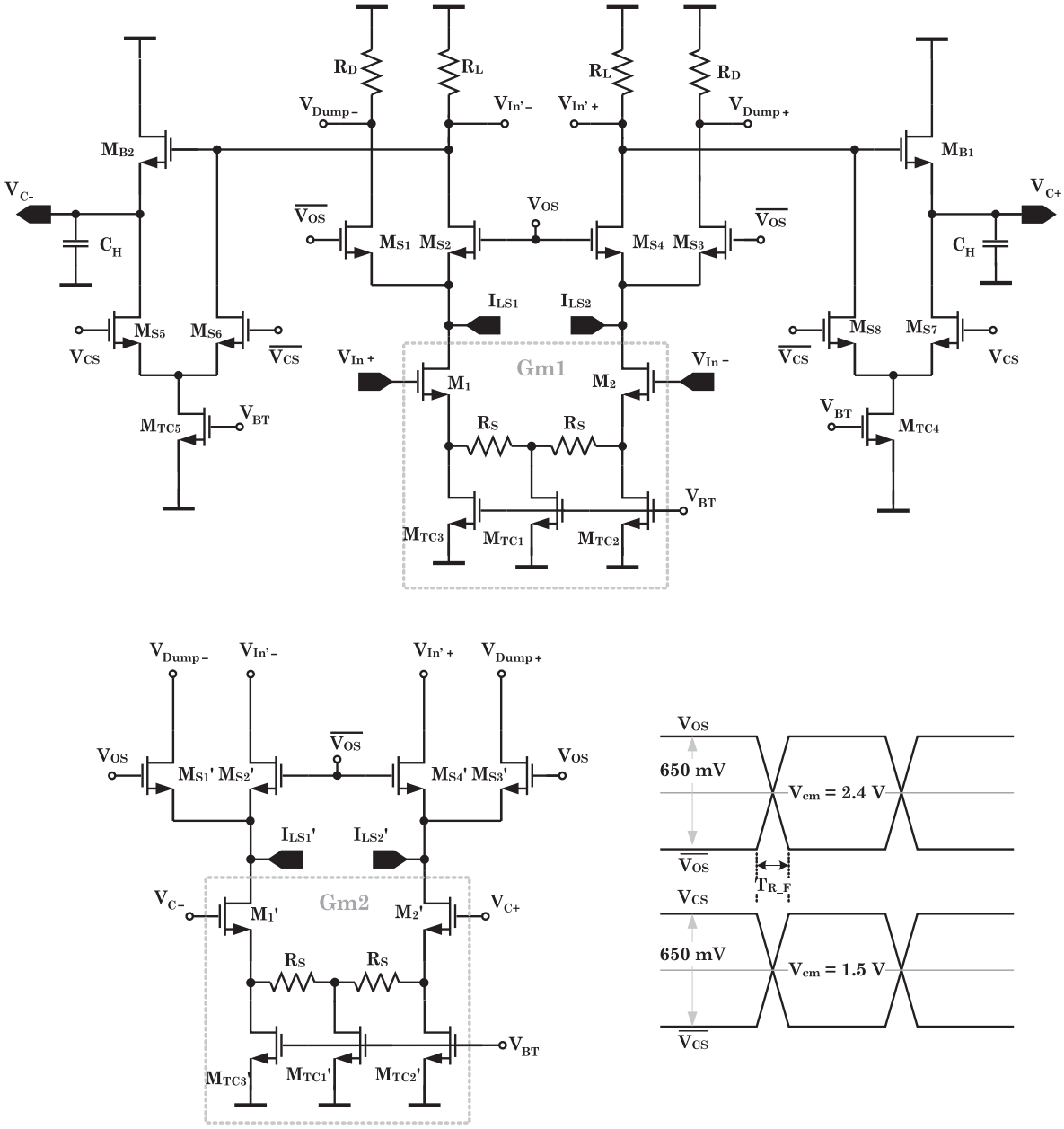


Figure 19: Simplified schematic of the proposed SHA along with the clocks necessary for proper operation. The clock signals have 650 mV_p signal swing.

Table 2: Transistor Aspect Ratios and Component Values for the Schematic Given in Figure 19

$\mathbf{M_1}$	$\mathbf{M_2}$	$\mathbf{M_{1'}}$	$\mathbf{M_{2'}}$	$\mathbf{R_S}$	$\mathbf{R_L}$
384/0.4	384/0.4	384/0.4	384/0.4	75	100
$\mathbf{M_{S1}}$	$\mathbf{M_{S2}}$	$\mathbf{M_{S3}}$	$\mathbf{M_{S4}}$	$\mathbf{M_{S5}}$	$\mathbf{M_{S6}}$
192/0.35	192/0.35	192/0.35	192/0.35	192/0.35	192/0.35
$\mathbf{M_{S1'}}$	$\mathbf{M_{S2'}}$	$\mathbf{M_{S3'}}$	$\mathbf{M_{S4'}}$	$\mathbf{C_H}$	$\mathbf{R_D}$
192/0.35	192/0.35	192/0.35	192/0.35	1p	100
$\mathbf{M_{B1}}$	$\mathbf{M_{B2}}$	$\mathbf{M_{TC1}}$	$\mathbf{M_{TC2}}$	$\mathbf{M_{TC3}}$	$\mathbf{M_{TC1'}}$
180/0.35	180/0.35	480/0.5	480/0.5	480/0.5	480/0.5
$\mathbf{M_{TC2'}}$	$\mathbf{M_{TC3'}}$	$\mathbf{M_{TC4}}$	$\mathbf{M_{TC5}}$		
480/0.5	480/0.5	600/0.5	600/0.5		

4.3.1 Input Buffer

As the name implies, the input buffer buffers the input voltage and isolates the source from the kick-back caused by the switching action. Furthermore, the input buffer implicitly facilitates the switching of the switched buffer, as the current through the switching buffer is steered to the load resistors of the input buffer. A source-degenerated cascode differential pair with resistive loads was used as the input buffer even though it has limited signal headroom. The transistors M_{S1-4} facilitate switching by steering the current from the actual loads to the dummy loads besides cascoding the input differential pair.

The nonlinearity of the input buffer is dominated by the input differential pair. The third-harmonic distortion of a differential pair with perfectly matching transistors is given by

$$\mathrm{HD3} = \frac{1}{32}\frac{1}{(1+\mathrm{T})^3}\left(\frac{\mathrm{V_d}}{\mathrm{V_{od}}}\right)^2, \tag{2}$$

where V_d is the peak value of the differential input voltage, V_{od} is the over-drive voltage of the input differential pair, and T is the loop gain ($T = gmR_S$ and R_S is the source degeneration resistance.) Equation 2, predicts the third harmonic distortion accurately at low frequencies. At high frequencies, Volterra analysis can be used for more accurate results, [49]. To get 70 dB SFDR with 250 mV_p input differential voltage and 150 mV overdrive, T has to be 5.5.

The gain and bandwidth (BW) requirements can be used to calculate the transconductance (gm) of the input differential pair and the value of the source-degeneration resistance (R_S.) The gain of the input buffer (A) is given by Equation 3, and its BW is given by Equation 4.

$$A = \frac{gmR_L}{1+T} \tag{3}$$

and

$$BW = \frac{1}{2\pi R_L C_L}, \tag{4}$$

where R_L is the load resistance and C_L is the total capacitance seen by R_L. The value of A has to be about 1.3 to have unity gain from the input to the hold node to account for the loss across the source follower, which has a gain of about 0.7-0.8. The significance of having a unity gain from the input to the hold node in terms of the value of hold pedestal is explained in Section 4.2. During design phase, the value of C_L was iterated to account for the layout parasitics. The final value of R_L was chosen as 100 Ω. The value of gm can be calculated by plugging the values of R_L and T into

Equation 3:

$$1.3 = \frac{\mathrm{gmR_L}}{1 + 5.5} \longrightarrow \mathrm{gm} = \frac{1.3 \times 6.5}{100} \approx 85 \text{ mA/V}. \tag{5}$$

Once the value of gm is known, the value of $\mathrm{R_S}$ can be calculated using the value of T:

$$\mathrm{T} = \mathrm{gmR_S} \longrightarrow \mathrm{R_S} = \frac{5.5}{0.085} \approx 65 \ \Omega. \tag{6}$$

With these values in hand, the electrical design of the input buffer is defined. The aspect ratios of the transistors used in the input buffer are tabulated in Table 2. The analog supply voltage was chosen to be 3.3 V to maximize dynamic range. Therefore, the thin-oxide input transistors $\mathrm{M_1}$, $\mathrm{M_1'}$, $\mathrm{M_2}$, and $\mathrm{M_2'}$ are cascoded by the thick-oxide switch transistors $\mathrm{M_{S1}} - \mathrm{M_{S4}}$ and $\mathrm{M_{S1}'} - \mathrm{M_{S4}'}$.

4.3.1.1 Tail Current Source

The tail current source of the input buffer is comprised of three transistors, $\mathrm{M_{TC1}} - \mathrm{M_{TC3}}$, see Figure 19. If the sizes of transistors $\mathrm{M_{TC2-3}}$ are maximized while keeping the total size of these three transistors constant, the signal handling capability is maximized. However, this approach has several adverse effects. First, the drains of $\mathrm{M_{TC2-3}}$ experience significant signal swing. Since the output impedance of the current sources formed by $\mathrm{M_{TC2-3}}$ are relatively small and nonlinear, the bias currents of the input transistors $\mathrm{M_{1-2}}$ vary with the input. On the other hand, input-dependent bias currents induce nonlinearity. Furthermore, significant parasitic capacitance is added to the sources of the input transistors $\mathrm{M_{1-2}}$. If the transistors $\mathrm{M_{TC2-3}}$ are quite

large, the added parasitic capacitances may result in peaking in the step response and increase settling time.

On the other hand, maximizing the size of M_{TC1} limits the signal handling capability drastically. However, this choice reduces the input-depended bias-current modulation. Furthermore, CM to DM conversion resulting from the finite output impedance and mismatch associated with M_{TC2-3} is smaller. Considering these factors, the sizes of $M_{TC1} - M_{TC3}$ were designed to be equal.

4.3.1.2 Common-Mode Adjustment

The output CM of the SHA was designed to be about 1.3 V, which is same as the input CM value. Therefore, same input CM is ensured for both the input buffer and the auxiliary buffer. Level shifting currents are injected at the nodes I_{LS1} and I_{LS2} to sustain the output CM around 1.3 V regardless of the values of the tail current R_L and supply voltage. The level shifting currents could be injected at the output of the input buffer. However, in that case, substantial nonlinear junction capacitances would be introduced to these nodes, which reduce BW and increase distortion. The schematic of the level-shifting current sources are given in Figure 20.

4.3.2 Switching Buffer

The switching buffer, which is comprised of transistors M_{B1-B2}, cascades the input buffer. The switching buffer is a source follower that can be switched on and off by steering its bias current with transistors M_{S5-8}. Steering the bias current of the buffer transistors from their sources to their gates generates a constant gate to source voltage (V_{GS}) shift of $I_{Tail} \times R_L$, which is independent of the input signal. This in

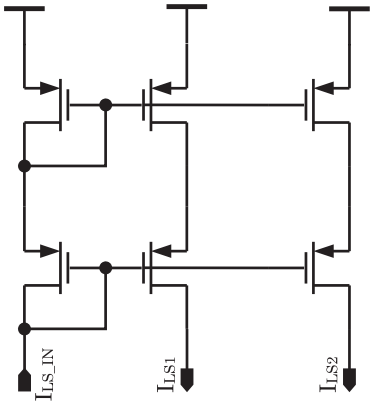


Figure 20: Schematic of the level shifting current sources.

turn, generates a bootstrapped clock signal. Hence, the switched-buffer SHAs have built-in bootstrapped clock. The track-mode SFDR of this stage was designed to be 70 dB. The second and third harmonic distortion of a source follower as a function of overdrive voltage, load current, and various parameters are expressed in Equations 7 and 8, where γ is the body-effect coefficient, Φ_F is the Fermi level in the substrate, V_{CM} is the CM voltage at the source terminal, Z_L is the load impedance, I_D is the drain current, A is the amplitude of the input signal and V_{od} is the overdrive voltage.

$$\mathrm{HD2} = \frac{\mathrm{A}}{16}\frac{\dfrac{\gamma}{\sqrt[3]{2\Phi_\mathrm{F}+\mathrm{V_{CM}}}}+\dfrac{\mathrm{V_{od}}}{(\mathrm{Z_L I_D})^2}}{\left(1+\dfrac{\gamma}{2\sqrt{2\Phi_\mathrm{F}+\mathrm{V_{CM}}}}+\dfrac{\mathrm{V_{od}}}{2\mathrm{Z_L I_D}}\right)^2} \tag{7}$$

$$\begin{aligned}\mathrm{HD3} =& \frac{\mathrm{A}^2}{64}\left[\frac{\left(\dfrac{\gamma}{\sqrt[3]{2\Phi_\mathrm{F}+\mathrm{V_{CM}}}}+\dfrac{\mathrm{V_{od}}}{\mathrm{Z_L I_D}}\right)^2}{\left(1+\dfrac{\gamma}{2\sqrt{2\Phi_\mathrm{F}+\mathrm{V_{CM}}}}+\dfrac{\mathrm{V_{od}}}{2\mathrm{Z_L I_D}}\right)^2}\right. \\ & \left. -2\frac{\dfrac{\gamma}{\sqrt[5]{2\Phi_\mathrm{F}+\mathrm{V_{CM}}}}+\dfrac{\mathrm{V_{od}}}{(\mathrm{Z_L I_D})^3}}{\left(1+\dfrac{\gamma}{2\sqrt{2\Phi_\mathrm{F}+\mathrm{V_{CM}}}}+\dfrac{\mathrm{V_{od}}}{2\mathrm{Z_L I_D}}\right)^3}\right]\end{aligned} \tag{8}$$

The value of the hold capacitor has several effects on the track- and hold-mode distortion. As the value of the hold capacitor increases, the current modulation experienced by the source follower increases. When the current modulation increases, distortion increases. The amount of current modulation should be limited below a certain level to achieve a desired level of SFDR. This implies that the value of the load impedance should be kept below a particular value. This constraint dictates that the hold capacitor must be below a certain value. Because of the pseudo-differential architecture of the circuit, the second harmonic distortion is significantly attenuated. Hence, it was not considered in determining the maximum value of the hold capacitor. For an easy estimation of the maximum value of the hold capacitor, the value of Z_L is changed and the result is plotted in Figure 21 along with the simulation results. In this simulation, the source follower was loaded with a resistor and the value of the load resistor was swept from 100 Ω to 500 Ω. The solid lines correspond to Equation 7 and 8. The dots on the other hand are simulation results (the second harmonic distortion is provided for the sake of completeness). As seen from Figure 21, to have about 70 dB SFDR, the impedance of the hold capacitor should be limited to about 180 Ω. With 500 MHz input frequency, the maximum value of the hold capacitor must be smaller than 1.77 pF, see Equation 9.

$$C_H < \frac{1}{2\pi f \times 180} \approx 1.77 \text{ pF}. \tag{9}$$

Smaller values of hold capacitance results in larger bandwidths and reduces distortion in the track mode. On the other hand, distortion in the hold mode reduces as the value of the hold capacitor increases. For instance, the hold pedestal reduces as the value of the hold capacitor increases. Similarly, switching-induced perturbations in the held voltage reduce as the value of the hold capacitor increases. Considering these factors, the value of the hold capacitor was chosen as 1 pF.

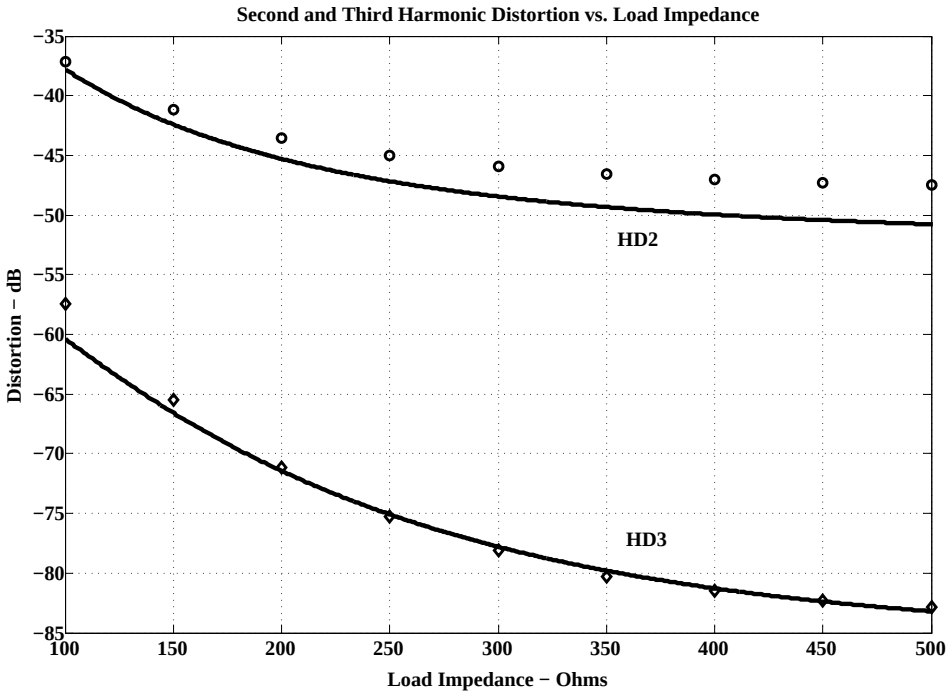


Figure 21: For an easy estimation of load impedance Equation 7 and 8 are plotted along with the simulation results (dots).

4.3.3 Auxiliary Buffer

The auxiliary buffer is essential for reducing hold pedestal and hold-mode distortion. As explained earlier the auxiliary buffer must be identical to the input buffer. Thus, all the design considerations that apply to the input buffer are valid for the auxiliary buffer.

4.3.4 Clock Buffer

The clock signals that switch the input and auxiliary buffers and the switching buffer, (V_{OS}) and (V_{CS}) respectively, were designed to keep the switch transistor in saturation when they are on. Furthermore, the transistors of the input differential pairs of the input and auxiliary buffers are always kept in saturation. Therefore, V_{OS} and V_{CS} are designed to have about 650 mV_{pp} signal swing with 2.4 V and 1.5 V_{CM} respectively. The clock signal waveforms are illustrated in Figure 19.

The sources of the switch transistors, $M_{S1} - M_{S4}$ and $M'_{S1} - M'_{S4}$, should be kept as quiet as possible to reduce the switching-induced distortion. This minimizes the adverse effects of the limited output impedance associated with the input transistors in the input and auxiliary buffer, and the tail-current transistors in the switching buffer. Keeping the sources of $M_{S1} - M_{S4}$ and $M'_{S1} - M'_{S4}$ quiet also reduces the transients caused by the charging and discharging of the capacitors associated with these source nodes. Consequently, the rising and falling edges of the clock signals should intersect somewhere close to the CM value of the associated clock signal. The rising and falling edges of the clock signals should also be as symmetrical as possible.

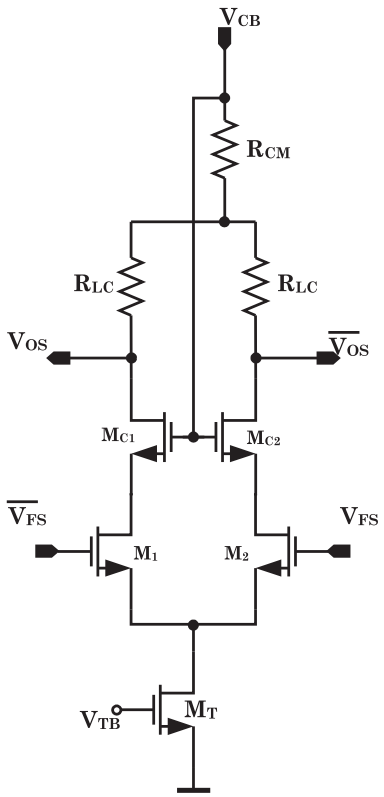


Figure 22: Source-coupled-logic buffer. M_{1-2} are thin-oxide devices, and M_{C1-2} are thick-oxide devices.

Table 3: Aspect Ratios of the Clock Buffer Transistors

$\mathbf{M_1}$	$\mathbf{M_2}$	$\mathbf{M_{C1}}$	$\mathbf{M_{C2}}$	$\mathbf{M_T}$	$\mathbf{R_{LC}}$	$\mathbf{R_{CM}}$
128/0.18	128/0.18	192/0.35	192/0.35	800/0.4	45	45

The clock signals with the aforementioned properties can be generated with differential pairs with resistive loads (source-coupled-logic -SCL- buffers), whose schematic is given in Figure 22. The aspect ratios of the transistors of the clock buffer are tabulated in Table 3. While the signal swing of the clock signals are determined by $I_{Tail} \times R_{LC}$, the CM voltages are given by $V_{CB} - I_{Tail}\,(R_{LC}/2 + R_{CM})$. The transistors M_1 and M_2 are 1.8 V devices. On the other hand, transistors M_{C1} and M_{C2} are thick-oxide transistors.

The SCL clock buffer is driven by full-swing 1.8 V digital signals. To obtain the

desired clock properties, the SCL clock buffer is driven by a latch, Figure 23, [50]. The output signals of this latch have relatively symmetric rising and falling edges. Moreover, the crossing point of the output signals, V_{FS} and $\overline{V_{FS}}$, can be designed to have a proper CM value by appropriately scaling the latch transistors. Properly designed CM voltage ensures that the tail-current transistor of the SCL buffer does not enter linear region during switching. Ensuring this improves the dynamic behavior of the SCL buffer. Finally, the latches driving various switches are clocked by a master clock (M-Clk) to synchronize the switching.

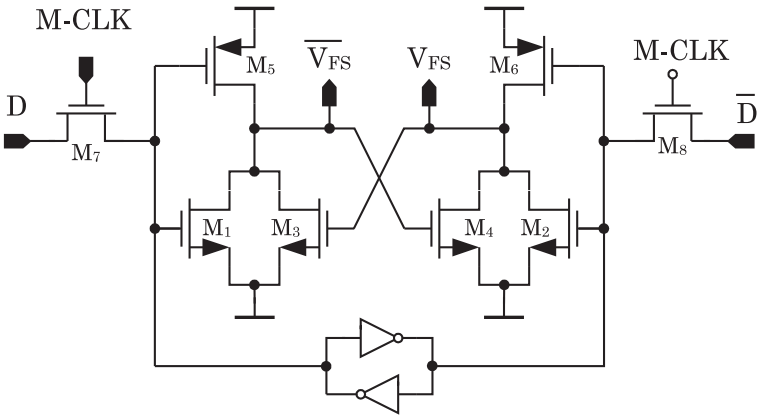


Figure 23: Schematic of the latch used to drive the SCL buffer.

Table 4: Aspect Ratios of the Transistors of the Latch Given in Figure 23

$\mathbf{M_1}$	$\mathbf{M_2}$	$\mathbf{M_3}$	$\mathbf{M_4}$
16/0.18	16/0.18	16/0.18	16/0.18
$\mathbf{M_5}$	$\mathbf{M_6}$	$\mathbf{M_7}$	$\mathbf{M_8}$
64/0.18	64/0.18	32/0.18	32/0.18

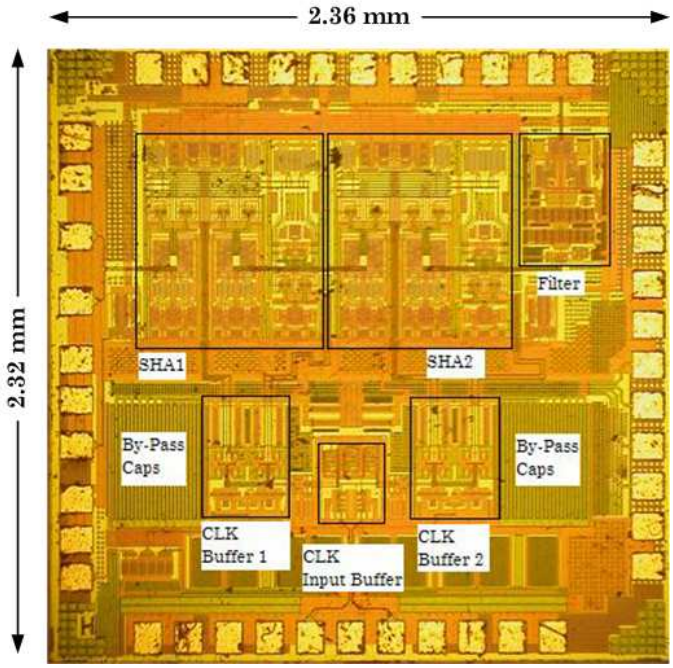
4.3.5 Output Buffer

The intended application of the designed SHA does not explicitly require an output buffer. Therefore, an output buffer was not designed. However, if desired, an output

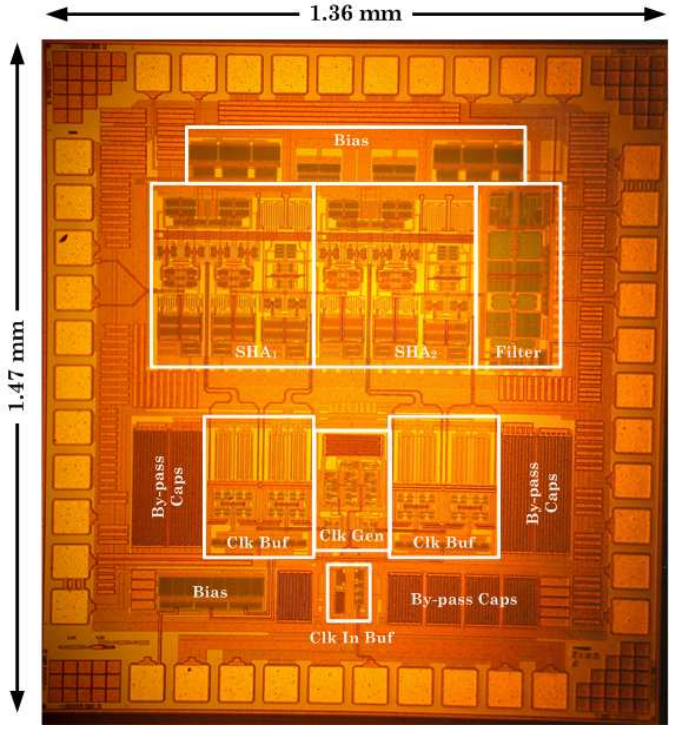
buffer like the one reported in [5] can be used. The linearity of the stages used in the output buffer can be optimized using Equation 2 and 8. An output buffer, which is capable of driving a load-capacitor same as the hold-capacitor, increases the power consumption by about 50 %.

4.3.6 Layout Considerations

Layout design is as important as the circuit design for high-frequency operation. Common centroid layout techniques were used throughout the design to minimize systematic offset. Further, the differential signal paths were equalized by making their lengths equal. Analog signal paths were shielded to balance the parasitic interconnect capacitance associated with these paths. Excessive shielding practice followed in the first chip's layout resulted in a large layout, which degraded high-frequency performance. As a result, shielding of signal paths was kept at a modest level in the second chip. Because of this, the size of the second chip is only about 60% of the first chip. The die photographs of the first and second chip are provided in Figure 24(a) and 24(b) respectively.



(a)



(b)

Figure 24: Die photographs. (a) Die photograph of the first SHA chip. (b) Die photograph of the second SHA chip.

4.4 Simulation and Experimental Results

Two different chips were fabricated to demonstrate the presented method. As mentioned in the previous section, extensive shielding was used to maintain signal integrity in the first chip. As a result, the layout turned out to be larger than expected. Therefore, layout parasitics degraded the high-frequency operation. In the second chip, the conservative shielding approach followed in the first chip was relaxed and the differential clock input used in the first chip was replaced by a single-ended clock input.

The classical re-sampling technique was used to characterize the performance of the SHA chips [5]. Thus, prototype chips consist of two SHAs. A low-pass filter was also integrated along with two SHAs. For the sake of brevity, the block diagram of the test setup of only the second chip is given in Figure 25(a). The second SHA on the chip runs at half the clock rate of the first SHA. As a result, if the input signal is at a frequency, which is close to the Nyquist rate of the first SHA, the second SHA down converts the output of the first SHA to low frequency. After filtering with sufficient bandwidth, the output of the second SHA can be used to characterize the performance of the first SHA. The frequency translation in the re-sampling technique is shown in Figure 25(b). The test setup of the first chip is same as the second chip, except for a minor difference: the first chip uses a differential clock signal. The simulated BW of the on board filters are about 10 MHz and 1 MHz for the first and second chips respectively. A clock-generator circuit, which generates the proper clock phases for the two SHAs, was also designed and integrated with the SHAs. The external,

sinusoidal clock signal is amplified and divided by 2 to get 50 % duty cycle. Thus, the external clock frequency is twice the sampling rate. The differential signals were generated from single-ended signals by transformers. The differential output signal was also converted to a single-ended signal by a transformer. The input signal was low-pass filtered to attenuate the harmonics of the signal generator.

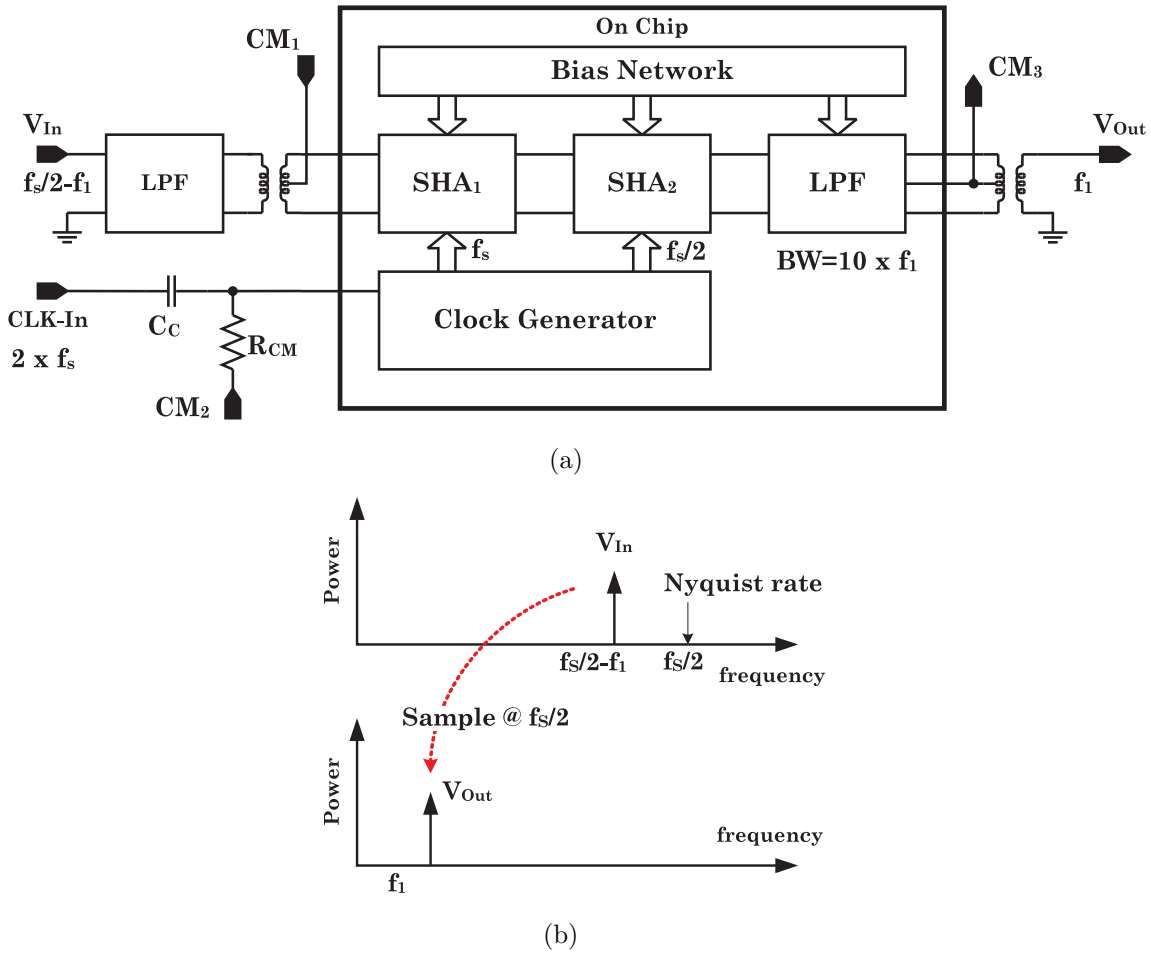


Figure 25: Test setup for the SHA chip. (a) Block diagram. (b) Demonstration of frequency translation with re-sampling method.

The transient response of the SHA could not be measured directly, however a simulation result is provided in Figure 26. In this simulation, the sampling frequency was 1 GHz, and the input differential signal had 500 mV_{pp} amplitude and 490.2344

MHz frequency. The simulated hold pedestal is about 1 mV. The measured spectra of the output signals are provided in Figure 27(a) and 27(b) for the first and second chip respectively. For these measurements, sampling frequencies were 1 GHz. The input amplitude was 400 mV_{pp}, and the frequencies of the input signals were 499.9 MHz and 500.1 MHz for the first and second chip respectively. Thus, the output were 100 KHz sinusoidal signals. Note that, the BW of the output filters were designed to be much larger than the frequency of the output.

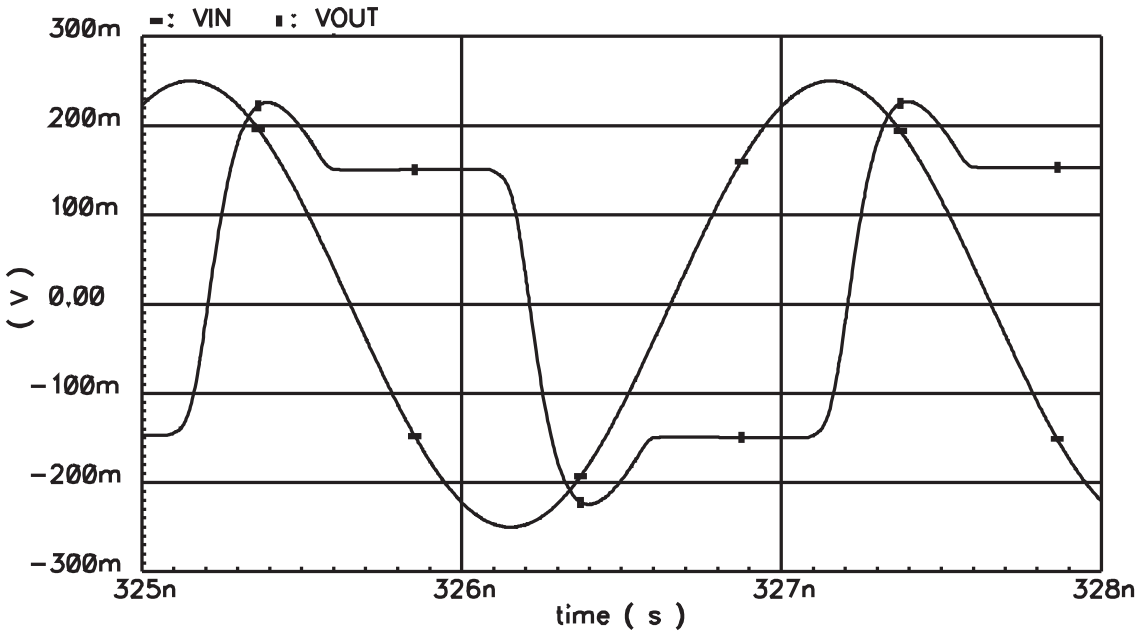


Figure 26: Simulated transient response of the SHA. In this simulation, the input was a 490.23 MHz, 500 mV_{pp} differential signal. Sampling frequency was 1 GHz.

The second, third, and total harmonic distortion observed at the output versus the sampling frequency are provided in Figure 28(a) and 28(b) for the first and second chip respectively. The output exhibits significant second harmonic content. When a single SHA was simulated, no even harmonics were observed in the spectrum of the output of the SHA. This is expected with the perfectly matching devices used

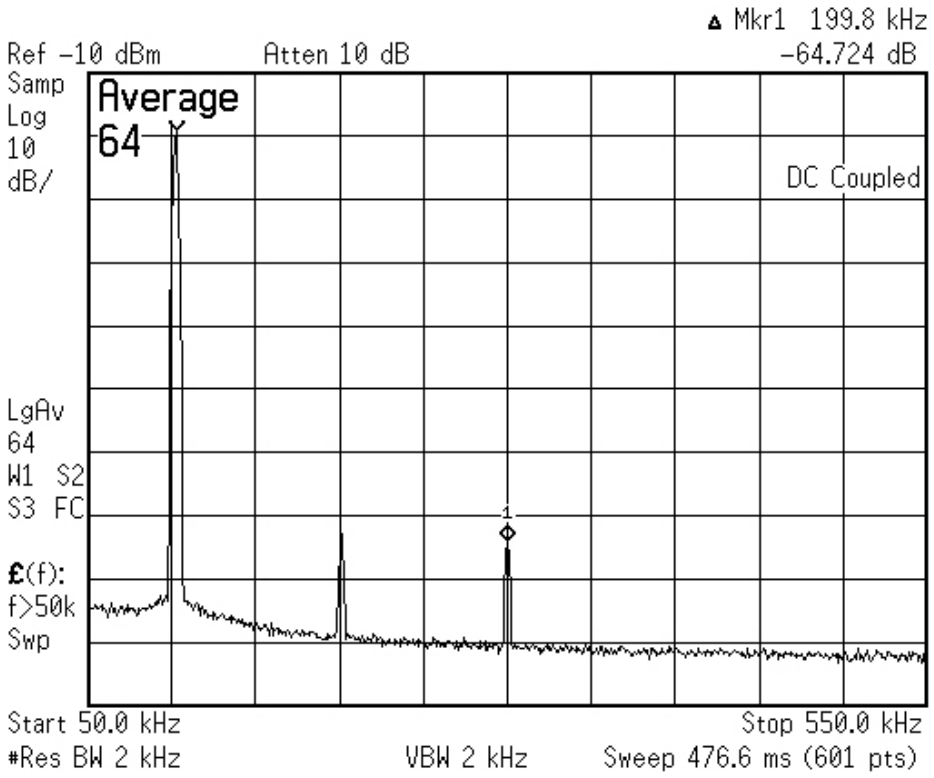
by the simulator. However, when two SHAs were simulated in the double sampling configuration, as depicted in Figure 25, second harmonic distortion was observed in the output spectrum. Since the input buffer used in the SHA exhibits very limited CM rejection, the second harmonic at the simulated output spectrum is caused by the modulation of the tail current of the input buffer of the second SHA by the common mode variation at the output of the first SHA. The imbalance in the transfer characteristic of the transformer and mismatch in the differential structure of the SHAs can worsen second harmonic distortion, during testing.

Nonetheless, the first chip has better than 62 dB SFDR up to 1.1 GHz sampling rate. On the other hand, the second chip has better than 62 dB SFDR up to 1.6 GHz sampling rate. In these measurements, the input signal amplitude was 400 mV_{pp}, and the input frequency was 100 kHz less (or more) than the Nyquist rate. A plot of the second and third harmonic distortions, and SFDR versus input level, for the second chip, is given in Figure 29. The performances of the designed SHA chips are tabulated in Table 5. Finally, the PCBs of the two chips are shown in Figure 30(a) and 30(b) respectively.

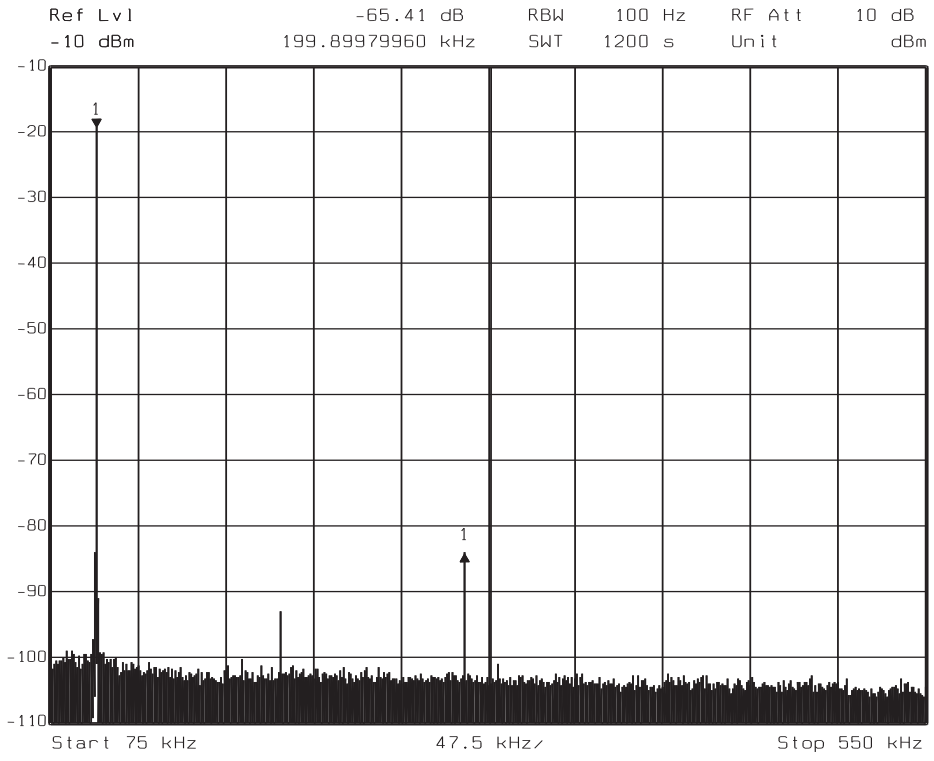
Table 5: Performance Summary of the Designed SHA Chips

Specification	**Comment**	**Chip1**	**Chip2**
Process	CMOS	0.18 μm	
Supply Voltage	Digital	1.8 V	
	Analog	3.3 V	
Analog Input	–	400 mV_{pp}	
Max. Clock Freq.	–	1.1 GHz	1.6 GHz
SFDR	400 mV_{pp} Input	$>$ 62 dB	
THD	400 mV_{pp} Input	$\leq$ -60 dB	
Power Dissipation	Single SHA	150 mW *	183 mW *
	Clock Buffer Without CMOS Logic	100 mW	75 mW
Area	Single SHA	0.7×0.8 mm^2	0.38×0.52 mm^2
Chip Area	–	2.36×2.32 mm^2	1.47×1.36 mm^2

* With an output buffer, the power consumption will increase by 50 %.

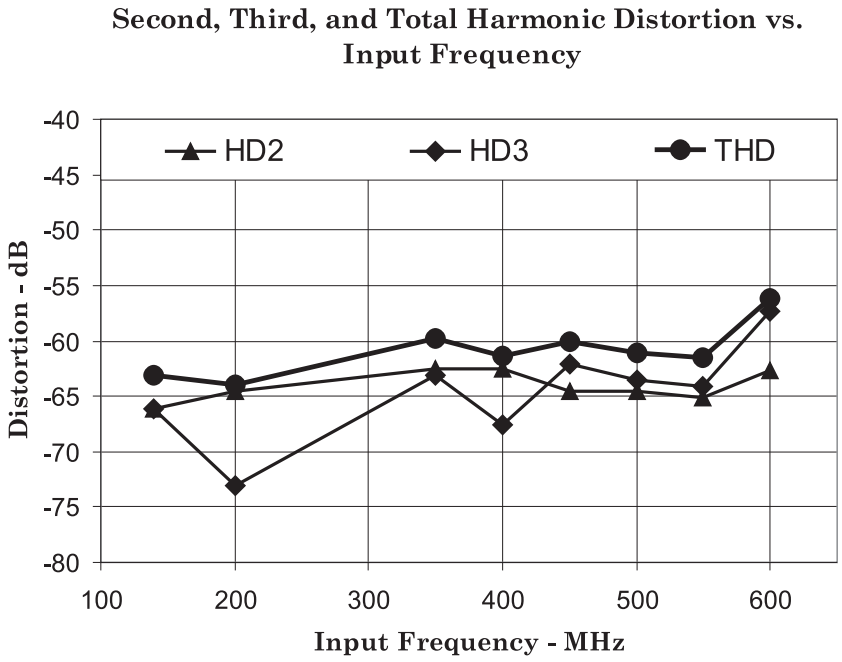


(a)

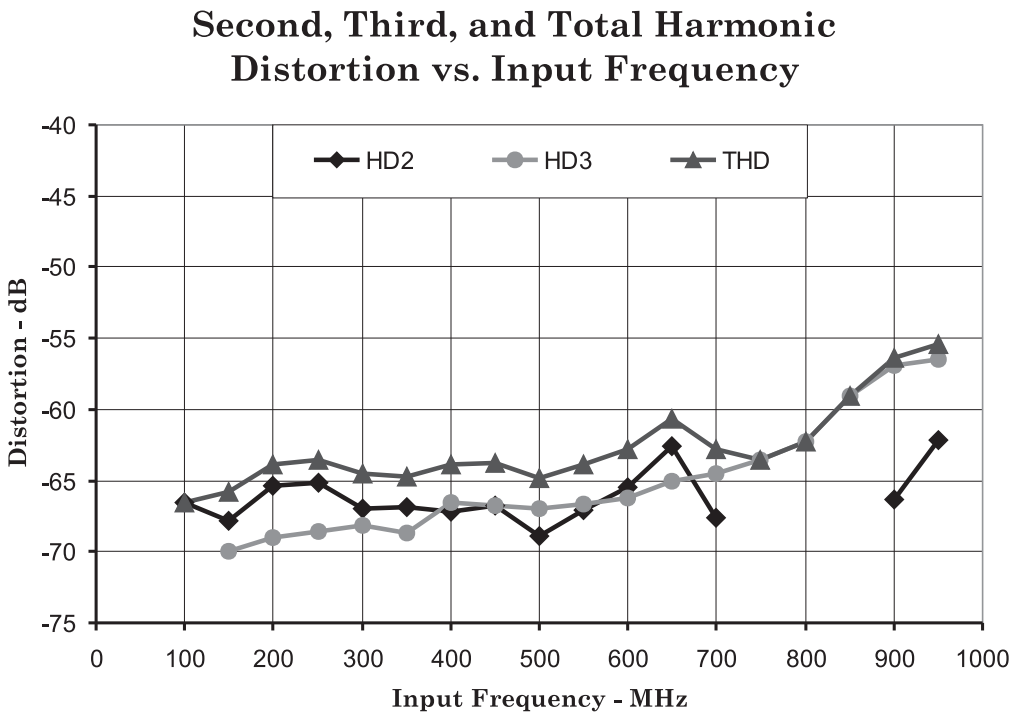


(b)

Figure 27: The spectrum of the output signal, with a 0.4 V_{pp} input signal. (a) For the first chip, with 499.9 MHz input signal at a sampling frequency of 1 GHz. (b) For the second chip, with 500.1 MHz input signal at a sampling frequency of 1 GHz.



(a)



(b)

Figure 28: The second and third harmonic distortion versus input frequency sampled at Nyquist rate. (a) Results for the first chip. (b) Results for the second chip. At the missing data points, corresponding harmonic was below the noise floor.

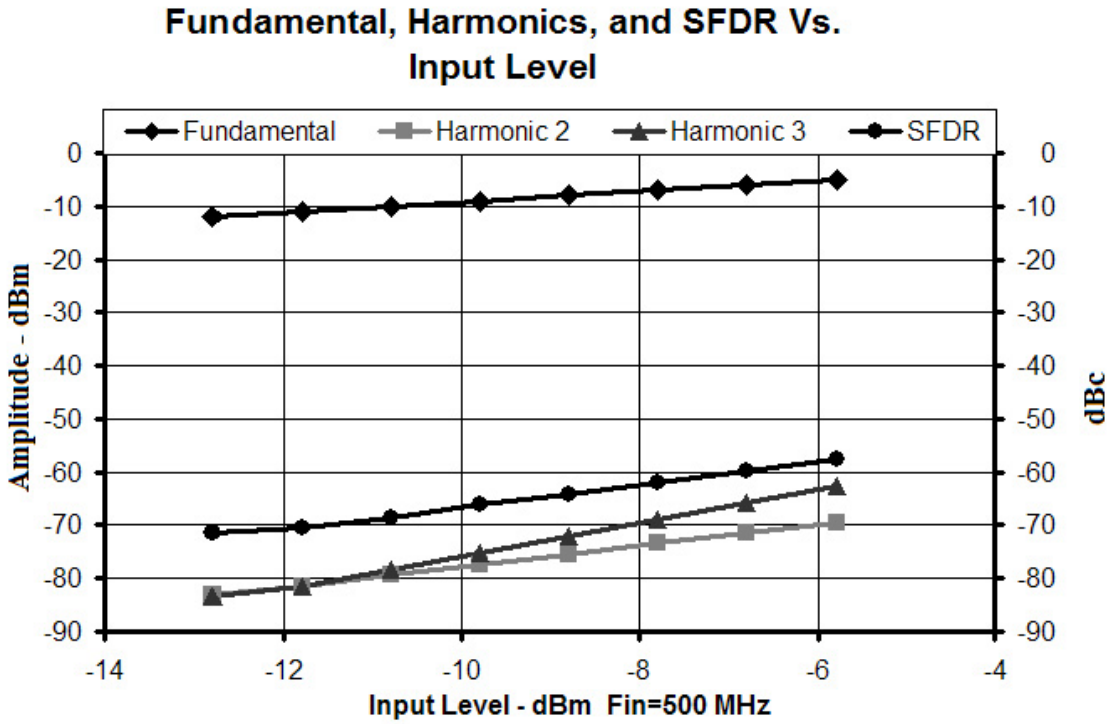
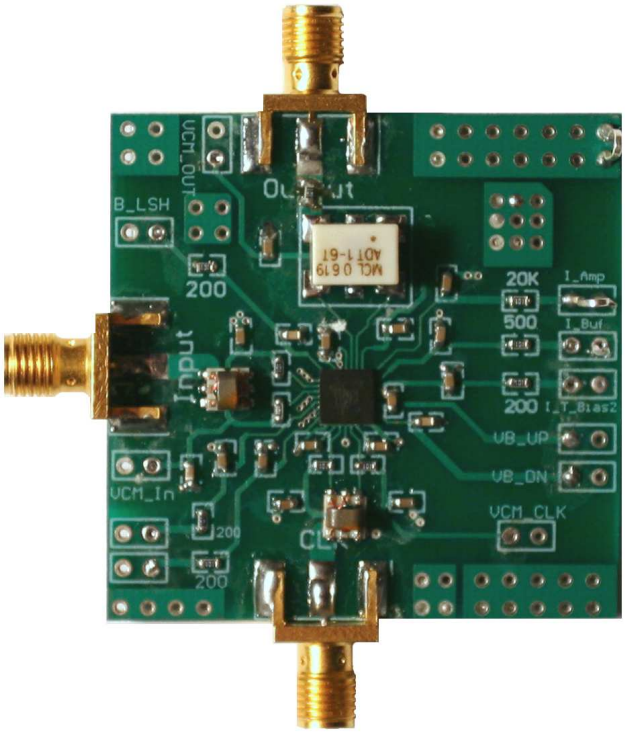
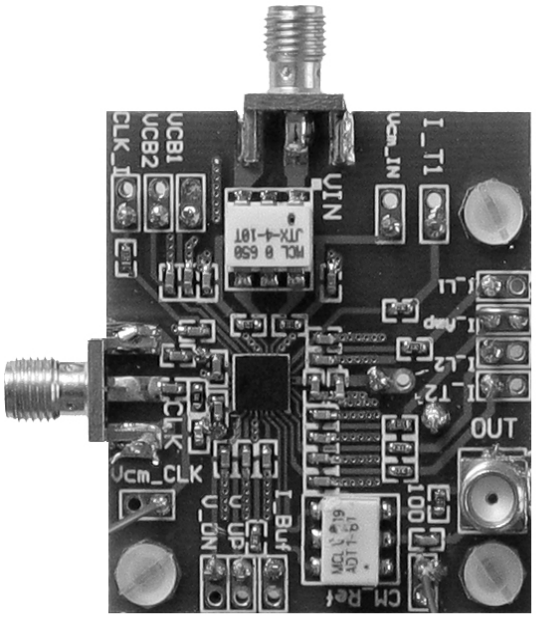


Figure 29: SFDR versus input level for the second chip with 500 MHz input frequency sampled at Nyquist rate.



(a)



(b)

Figure 30: Photographs of the PCBs used in testing. (a) PCB of the first chip. (b) PCB of the second chip.

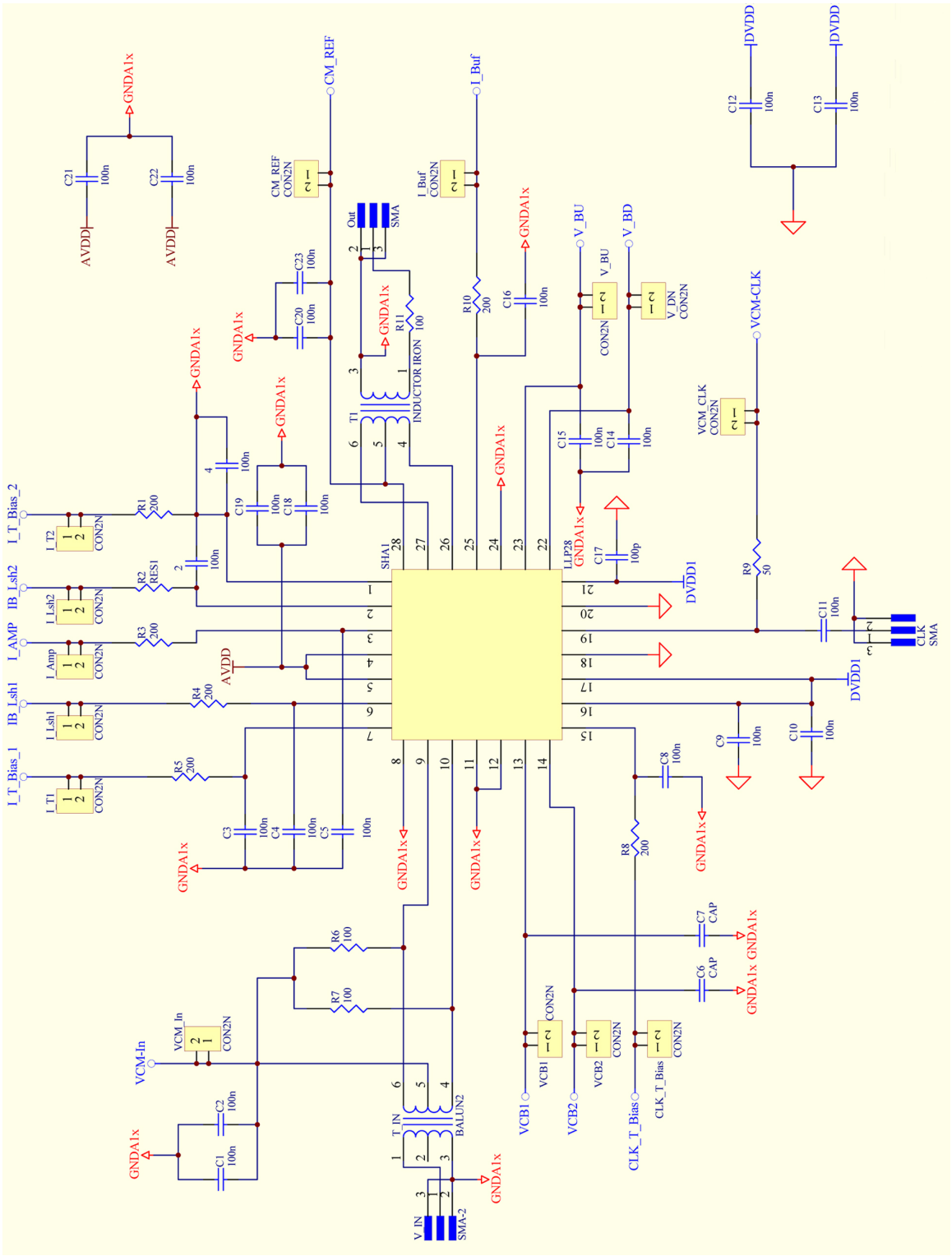


Figure 31: Schematic of the PCB used for testing.

4.5 Summary

The modularity of the two-step pipelined ADC architecture makes it the best candidate for high-speed operation with relatively high resolutions. Two-step pipelined ADCs have to incorporate high-performance SHAs to facilitate pipelining and alleviate clock- and signal-routing problems. For high sampling rates, active CMOS SHAs are not suitable because of the global-feedback OTAs used in these architectures. Further, even though the switched-buffer SHA topology suits best for two-step pipelined ADCs, the performance of the classical switched-buffer architecture deteriorates at high input frequencies.

In this chapter, a double-switching SHA is described. The double-switching technique provides two levels of isolation from the input to the sampled voltage, and eliminates the hold-mode feed-through problem in switched-capacitor SHAs. As a result, the linearity is sustained with input frequencies up to the Nyquist rate. The double-switching SHA architecture removes one of the major bottle necks in the design of high-speed two-step ADCs. The designed CMOS SHA is comparable to previously reported bipolar SHAs both in accuracy and sampling rate. A comparison of the designed chips with other work is given in Table 6

The proposed double-switching architecture resulted in significant power and area savings compared to the architecture reported in [47]. Compared to classical switched-buffer SHAs, double-switching switched-buffer SHA architecture requires an auxiliary transconductor stage. Consequently, the power dissipation of the double switching architecture is about 30 % larger than the classical switched buffer SHA.

As a conclusion, the switched-buffer SHA topology is more suitable for bipolar technologies. The significance of the proposed SHA architecture is already understood by the authors of [51], and it is replicated in their system in a bipolar process.

Table 6: Performance Comparison of Switched-Buffer SHAs

ENOB	$\mathbf{F_S}$ **(MHz)**	$\mathbf{F_{In}}$ **(MHz)**	$\mathbf{V_{FS}}$ **(V)**	$\mathbf{V_{Sup}}$ **(V)**	**P (mW)**	**Technology**	**Ref**
9.6	1100	550	0.4	3.3	150 *	0.18 μm CMOS	Chip I
10	1200	600	0.4	3.3	183 *	0.18 μm CMOS	Chip II
10	120	60	1	-5	40	Bipolar	[5]
10	185	45	1	3.3	70	0.35 μm CMOS	[6]
10	1000	500	1	-5.2	350	0.4 μm Bipolar	[47]
10.5	300	50	0.5	2.7	30	0.5 μm BiCMOS	[46]
10	250	100	1	5	225	BiCMOS	[52]
8.4	1200	600	1	$+2/-5$	460	Bipolar	[53]
6.5	4000	10000	2	5.2	550	Si/SiGe	[43]

* With an output buffer, the power consumption will increase by 50 %.

CHAPTER V

TWO-STEP PIPELINED ANALOG-TO-DIGITAL CONVERTER WITH OPEN-LOOP RESIDUE AMPLIFICATION

Operating speed of global-feedback circuits are limited by their stability requirements. We propose a two-step ADC, which makes use of local feedback and current-mode signal processing to alleviate the speed limitations caused by the stability requirements. The shortcomings of the local feedback circuits used in the design are compensated by exploiting the benefits of the selected ADC architecture and utilizing background calibration. The design consists of 2 stages, each of which has 5-bit resolution. The simplified block diagram of the proposed ADC is given in Figure 32. There are two SHAs in the proposed ADC. A SHA is used as a front-end SHA to alleviate timing mismatches at the input of the first stage (Stage1). Another SHA is used in Stage1 to pipeline the A/D and D/A conversion in this stage. A SHA is not necessary between Stage1 and the second stage (Stage2) as Stage2 is a simple flash ADC.

The number of stages that comprise a pipelined ADC and the resolution of these stages have profound effects on its power consumption, noise, and conversion speed [54]. Increasing the resolution of Stage1, typically, reduces the overall power consumption and noise. However, increasing the resolution of Stage1 aggravates its design because the accuracy requirements within a stage increases with increasing

stage resolution. This results from the reduction of the tolerable error range (which is commonly referred to as correction range) as the stage resolution increases. In other words, the offset limit of the ADC used in Stage1 reduces. Further, since an open-loop interstage amplifier is used in this design, a more linear interstage amplifier is required as the Stage1 resolution reduces. Moreover, choosing the Stage1 and Stage2 resolution to be the same reduces the design and layout effort. Considering the accuracy limits of the open-loop interstage amplifier used in this design and with the possibility of using the same 5-bit flash ADC in Stage1 and Stage2, the resolution of each stage is chosen as 5 bits.

With two 5-bit stages and one-bit error correction, the proposed ADC has 9-bit overall accuracy. Even though error correction relaxes the accuracy requirements of the blocks comprising the ADC, the gain and linearity of each block must be carefully optimized and controlled across process, supply voltage and temperature (PVT) corners. The details of the accuracy limits of the blocks comprising this design are discussed in the following section.

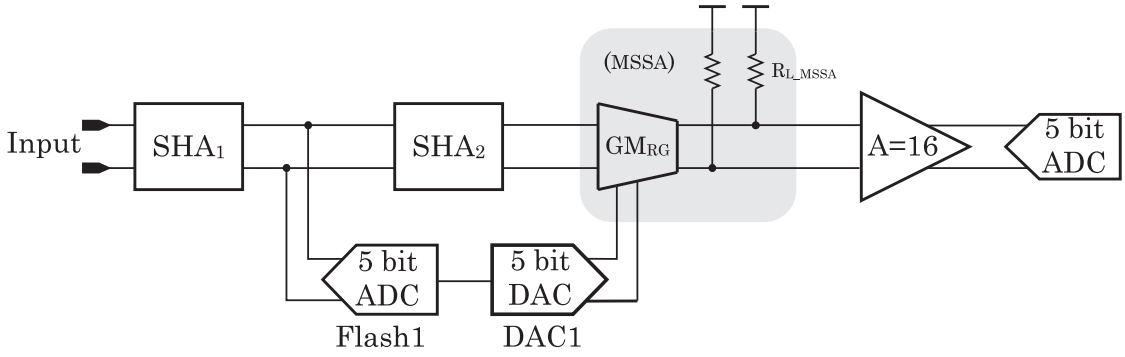


Figure 32: Block diagram of the proposed ADC.

5.1 Fundamental Design Requirements

Local feedback provides significant advantages in terms of bandwidth, power, and possibly area. With the use of local feedback, the complexity of the building blocks such as transconductance (Gm) stages also reduces. However, a heavy toll is paid in terms of increased susceptibility to PVT variations. The linearity of local-feedback circuits at low frequencies is generally worse than their global-feedback counterparts. Nonetheless, local feedback is sufficient to obtain the $60-66$ dB linearity required in this design. The linearity, gain accuracy, and input offset requirements of the blocks comprising a pipelined ADC are discussed in several references such as [1, 2]. For the sake of completeness the following section briefly summarizes these requirements for this design.

5.1.1 Nonlinearity Limits of the Building Blocks

The front-end SHA determines the linearity of the overall ADC. Therefore, it has to be at least 9-bit linear. This requirement is not relaxed by error correction. However, error correction relaxes the linearity requirement of the 5-bit ADC used in Stage1 (Flash1). Because of 1-bit error correction, Flash1 can be only 5-bit linear. On the other hand, for proper error correction the DAC in Stage1 must be 9-bit linear. Furthermore, SHA_2 must also be 9-bit linear. This also means that the residue generator block ($\mathrm{Gm}_{\mathrm{RG}}$ block in Figure 32) must be 9-bit linear. Finally, the residue amplifier and Stage2 must be only 5-bit linear. The linearity requirements discussed above are absolute limits for the corresponding block when others are perfectly linear. Consequently, linearity of each block has to be designed and optimized with some

safety margin.

5.1.2 Gain-Accuracy Requirements of the Building Blocks

The gains of the blocks comprising the ADC must remain within certain limits for proper operation. The gain variation of the front-end SHA simply introduces a global gain error. For most applications, a global gain error is not important. Typically, the input signal of an ADC is amplified to a few dB below its full-scale by a programmable-gain amplifier, which can compensate a global gain error. The gain variation of the blocks used in Stage1 can be absorbed by the accuracy requirement of Flash1 because of error correction. Therefore, error correction relaxes the gain-variation limits of the blocks comprising Stage1 significantly. This means that, gains of the blocks comprising Stage1 have to be only 5-bit accurate. However, the gain accuracies of the residue amplifier and Stage2 are not relaxed by error correction. They have to be as accurate as Stage2 (the back-end), which is 5-bit accurate. Similar to the linearity requirements, the gain accuracies discussed above are absolute limits of a particular block when others have ideal gain values. For the sake of completeness the linearity and gain-accuracy requirements of the blocks comprising the ADC shown in Figure 32 are tabulated in Table 7.

Table 7: Linearity and Gain-Accuracy Requirements of the Blocks Comprising the ADC of Figure 32

Block	**Linearity (bits)**	**Gain Accuracy (bits)**
SHA_1	9	–
SHA_2	9	5
Residue Generator	9	5
Interstage Gain	5	5
Flash1, Flash2	5	5
5-bit DAC	9	5

It is well known that the gain variation of a local-feedback circuit is more pronounced compared to a global-feedback circuit. This follows from the feedback theory:

$$\frac{\partial \mathrm{A}}{\mathrm{A}} = \frac{\partial \mathrm{a}/\mathrm{a}}{1+\mathrm{T}}, \tag{10}$$

where, **A** is the open-loop gain, **a** is the closed-loop gain, and **T** is the loop gain. As indicated in (10), variation in gain under closed-loop operation is reduced by the loop gain. This suggests that the variation gets smaller and smaller as the feedback (**T**) gets stronger and stronger. It can be shown that several other parameters are desensitized in a similar manner.

The main variation that deteriorates the performance of this design is gain variation caused by PVT changes. As far as gain accuracy is concerned, the interstage amplifier is the most susceptible stage to PVT changes because it has an open-loop topology. The gain variation due to different reasons and several possible methods to improve gain accuracy are discussed in the following.

5.1.2.1 Gain Variations Caused by Process Corners

It is expected that the device parameters can change up to ±30% across process corners. As mentioned earlier, the blocks comprising the proposed ADC utilizes local (or no) feedback. However, since local feedback (i.e. small **T**) makes the circuit more dependent on absolute device parameters, the gains of the building blocks can change significantly across process corners. Nonetheless, the variation in gain caused by process corners is constant after the chip is fabricated. As a result, gain variation caused by process corners can be compensated by trimming.

5.1.2.2 Gain Variations Caused by Supply-Voltage Variations

The variations in the supply voltage do not cause significant variations in gain. However, because of their topologies, the common-mode voltages of several stages are sensitive to supply voltage variations. Nonetheless, the supply-dependent common-mode voltages can be corrected by common-mode-feedback circuits. A more direct approach is followed in this design and the common-mode values of the SHA blocks are corrected with currents injected to the common sources of the current-steering switches as explained in Section 4.3.1.2.

5.1.2.3 Gain Variations Caused by Temperature Variations

The gain variations caused by temperature are the most catastrophic gain variations in this design. Therefore, various methods were investigated to alleviate these variations. Some of the significant methods investigated during the design phase are discussed briefly in this section. The detailed explanation of the proposed solution, however, is reserved for the following sections.

In this design, the SHAs, MSSA and interstage amplifier (with $R_S = 0$) depend on local feedback to sustain the designed gain. The gain of the local-feedback blocks used in this design (A_{local}) can simply be written as

$$A_{local} = \frac{g_m R_L}{1 + g_m R_S}. \tag{11}$$

It is apparent from Equation 11 that A_{local} can vary with temperature because of two reasons. The first reason is the variation in resistances, which define the gain and feedback factor. The second reason is the variation in transconductance.

The resistors used in this design are silicided poly resistors. The temperature coefficient (TC) of a silicided poly resistor is about +3000 ppm. The variation in transconductance depends on several transistor parameters such as mobility and threshold voltage (V_T). In this design, temperature dependence of V_T, which is about $-1, -2\text{mV/C}^\circ$, has a less significant effect on the gain because transconductances are defined by tail currents, [55–57]. However, mobility variations caused by temperature directly alters the gain.

The temperature induced variations in gains of the local feedback circuits used in this design can be compensated in several ways. The first way is to scale the gain of the DAC in accordance with the gain variations in SHA_2 and GM_{RG}, and change the reference of Stage2 to account for the gain variations in Stage1 and the interstage amplifier. However, this method is not practical because it involves changing the gain of the DAC and the reference of Stage2 to compensate the gain variations of several different blocks with at least 5-bit accuracy.

The second method is to cancel the gain variation of a particular block by adaptively changing its bias current as temperature changes. For example, simulations have shown that if the bias current of a Gm stage, such as the one used in the SHA or GM_{RG} block, has a TC of about -1000 ppm, the variation in its gain is compensated. However, this compensation is dependent on absolute device parameters, which are process dependent. Moreover, this compensation method fully depends on the accuracy of the device models. Thus, being an open-loop compensation technique, this temperature dependent adaptive biasing scheme is not practical without trimming. Even if the temperature variations of local feedback circuits are compensated their

absolute value must be trimmed or the reference of that stage must be scaled to compensate the absolute value shifts. On the other hand, changing the TC of the reference requires the correction of reference used in each stage, and should account for the gain variations of the previous stages as well as the gain variations caused in that stage. This requirement aggravates the correction scheme. Therefore, reference correction scheme becomes difficult for an ADC with more than 2 stages.

Another way to adaptively bias the blocks comprising the ADC is to use auxiliary blocks. The auxiliary blocks can be scaled replicas of their corresponding main blocks within the ADC. The gain of the auxiliary block can be compared with an accurate gain reference. The comparison result can be used to generate an error signal, which can vary the bias currents of the auxiliary and main blocks to compensate for any gain variations caused by temperature. Since the gain comparison can be done at low frequencies, the gain reference can be an accurate, global-feedback circuit. However, the auxiliary and main blocks reside at different locations on the die. As a result, the scaling factor between the main and auxiliary blocks depends on matching. Simulations have shown that mismatch between the auxiliary and its corresponding main block results in a gain offset. However, the temperature drift is compensated. This result is similar to gain variations due to process corners. Therefore, the gain shift can be corrected by trimming the references, and proper operation can be guaranteed as long as the temperature drift is low enough.

The gain variation in the interstage amplifier can be compensated by calibrating its gain in the background. The background calibration technique has been popular in the last 5-8 years and several different methods have been proposed. In this design,

we propose a background calibration technique, which scales the reference of Stage2 by the same factor that scales the gain of the interstage amplifier. The details of the proposed method, its variations, and several other recently reported background calibration methods are discussed in the following section. However, before explaining the details of the calibration method, the design considerations of the blocks comprising the ADC are discussed.

5.2 Building Blocks of the Proposed Analog-to-Digital Converter

In this section, the design considerations of the blocks comprising the proposed ADC are discussed in detail. As mentioned earlier, the proposed ADC consists of two stages, each of which has 5-bit resolution, Figure 32. With 1-bit error correction, the total design reduces to a 9-bit ADC. The design uses identical SHAs, two identical 5-bit flash ADCs, a 5-bit DAC, a residue generator, and an interstage amplifier.

5.2.1 Sample-and-Hold Amplifier

The proposed design employs a front-end SHA to alleviate timing and signal skew requirements. Another SHA is used for pipelining the input-sampling and residue-generation phases, see Figure 32. The front-end SHA can be omitted in a SHA-less design. However, a SHA-less implementation requires tight timing and group-delay matching between Flash1 and SHA_2. Because of the relatively high Stage1 resolution, the offset budget of the comparators used in Flash1 is relatively tight. Therefore, a front-end SHA is used to allocate all of the correction range for comparator offset. Note that, in a SHA-less front-end, some portion of the correction range has to be

allocated for timing and signal skews.

The schematic of the SHA is provided in Figure 19. The properties of the SHA and its design considerations are discussed earlier. Therefore, the design details of the SHA will not be discussed in this section. Nonetheless, the sensitivity of the gain of the SHA to various circuit parameters is given in Equation 12:

$$\begin{aligned}\frac{\sigma^2(\Delta A)}{A^2} = \frac{\sigma^2(\Delta R_L)}{R_L^2} + \frac{\sigma^2(\Delta gm_1)R_L^2}{(1+gm_1R_S)^2} + \frac{\sigma^2(\Delta R_S)gm_1^2}{(1+gm_1R_S)^2} \\ + \frac{\sigma^2(\Delta gm_2)gmb_2^2}{(gm_2+gmb_2)^2gm_2^2} + \frac{\sigma^2(\Delta gmb_2)}{(gm_2+gmb_2)^2},\end{aligned} \tag{12}$$

where A is the gain of the SHA, R_L is the load resistance, gm_1 is the transconductance of the input differential pair, R_S is the source degeneration resistance, gm_2 is the transconductance of the switching buffer, and gmb_2 is the back-gate transconductance of the switching buffer. The variation in gain due to PVT corners can be estimated by Equation 12.

5.2.2 5-Bit Analog-to-Digital Converter

The proposed ADC utilizes 2 identical 5-bit flash ADCs; one within Stage1 (Flash1) and the other as Stage2 (Flash2). As explained earlier, both of the 5-bit flashes must be only 5-bit accurate. Thus, their design is quite relaxed with only the input-referred offset remaining as a challenging design parameter. Since Flash1 and Flash2 are identical, their design considerations are discussed on a generic 5-bit flash ADC to simplify the arguments. This 5-bit flash ADC will be referred to as 5-bit flash in this section. The 5-bit flash utilizes a preamplifier block, which has 2 stages and a total gain of about 3.5. The pre-amplifiers reduce the input-referred comparator

offset and kick-back from the latches, and increase the sensitivity of the comparators [1, 56]. The block diagram of the 5-bit flash is given in Figure 33.

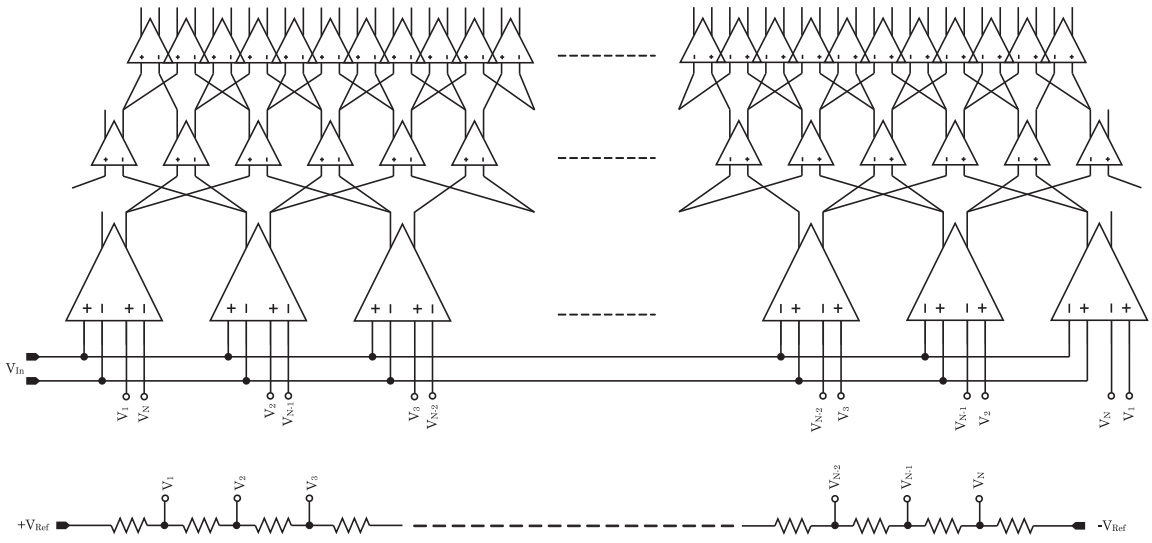


Figure 33: Block diagram of the 5-bit flash ADC.

The amplifiers comprising the first preamplifier stage are differential difference amplifiers, which compare the reference taps against the differential input signal, Figure 34(a). The amplifiers used in the second pre-amplifier stage are simple differential pairs with resistive loads, Figure 34(b). With 500 mV full scale, the input-referred offset requirement is 7.8125 mV. Averaging reduces the amplifier count and input-referred offset [16, 58]. Therefore, averaging is exploited to obtain the 7.8125 mV input-referred offset requirement. The outputs of the amplifiers comprising the pre-amplifier block are cross connected as shown in Figure 33. A few extra amplifiers must be used at the boundaries to equalize the loading. If the pre-amplifier loads are not equalized, the trip points of the comparators at the boundaries change because of comparator kick-back.

The averaging scheme utilized in the pre-amplifier block, averages the offsets of

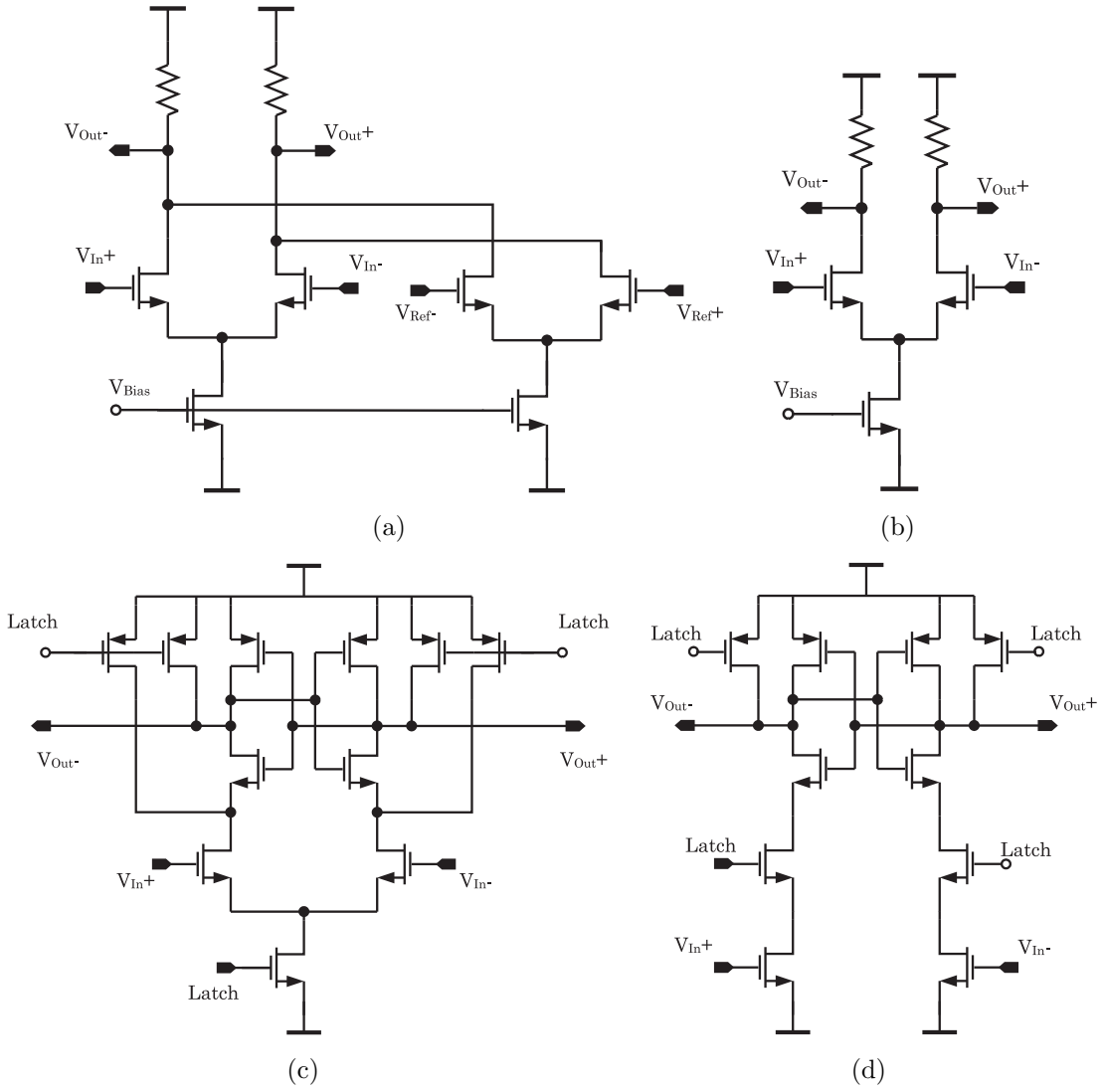


Figure 34: Building blocks of the 5-bit ADC. (a) Differential difference amplifier. (b) Differential amplifier. (c) Tail-latched dynamic comparator. (d) Classical dynamic comparator.

2 amplifiers from the second stage of the pre-amplifier block, Equation 13. Consequently, just because of averaging, the offsets of the amplifiers used in the second stage of the pre-amplifier stage are scaled by $\frac{1}{\sqrt{2}}$, Equation 14.

$$V_{Off} = \frac{V_{Off_i}}{2} + \frac{V_{Off_{i+1}}}{2} \tag{13}$$

$$\mathrm{E}\left[\mathrm{V}_{\mathrm{Off}}^2\right] = \frac{1}{4}\mathrm{E}\left[\mathrm{V}_{\mathrm{Off_i}}^2 + \mathrm{V}_{\mathrm{Off_{i+1}}}^2\right] = \frac{1}{2}\mathrm{E}\left[\mathrm{V}_{\mathrm{Off_i}}^2\right] \tag{14}$$

$$\sigma\left(\mathrm{V}_{\mathrm{Off}}\right) = \frac{1}{\sqrt{2}}\sigma\left(\mathrm{V}_{\mathrm{Off_i}}\right) \tag{15}$$

On the other hand, the input to a comparator is an average of 4 first-stage amplifier outputs. Depending on the location of the comparator on the averaging tree, all of these 4 amplifiers can be different or 2 of these 4 amplifiers can be same. This can be verified by inspecting the averaging tree depicted in Figure 33. If all of the 4 amplifiers are different, the offset of these amplifiers are attenuated by 2 as can be seen from Equations 16-18.

$$\mathrm{V}_{\mathrm{Off}} = \frac{\mathrm{V}_{\mathrm{Off_i}}}{4} + \frac{\mathrm{V}_{\mathrm{Off_{i+1}}}}{4} + \frac{\mathrm{V}_{\mathrm{Off_{i+2}}}}{4} + \frac{\mathrm{V}_{\mathrm{Off_{i+3}}}}{4} \tag{16}$$

$$\mathrm{E}\left[\mathrm{V}_{\mathrm{Off}}^2\right] = \frac{1}{4}\mathrm{E}\left[\mathrm{V}_{\mathrm{Off_i}}^2\right] \tag{17}$$

$$\sigma\left(\mathrm{V}_{\mathrm{Off}}\right) = \frac{1}{2}\sigma\left(\mathrm{V}_{\mathrm{Off_i}}\right) \tag{18}$$

If, on the other hand, 2 of these 4 amplifiers are same, then 2 of the 4 offset values are correlated. As a result, the offset of these amplifiers are attenuated by $\sqrt{6}/4$ as shown by Equations 19-21.

$$\mathrm{V}_{\mathrm{Off}} = \frac{\mathrm{V}_{\mathrm{Off_i}}}{2} + \frac{\mathrm{V}_{\mathrm{Off_{i+1}}}}{4} + \frac{\mathrm{V}_{\mathrm{Off_{i+2}}}}{4} \tag{19}$$

$$\mathrm{E}\left[\mathrm{V}_{\mathrm{Off}}^2\right] = \frac{6}{16}\mathrm{E}\left[\mathrm{V}_{\mathrm{Off_i}}^2 + \mathrm{V}_{\mathrm{Off_{i+1}}}^2\right] \tag{20}$$

$$\sigma\left(\mathrm{V}_{\mathrm{Off}}\right) = \frac{\sqrt{6}}{4}\sigma\left(\mathrm{V}_{\mathrm{Off_i}}\right) \tag{21}$$

Input-referred offset is a weighted sum of the comparator, second-stage preamplifier and first-stage amplifier offsets. The offsets of the second- and first-stage amplifiers are weighted by the averaging coefficients discussed above. Furthermore, any gain from the 5-bit flash input to the input of a particular block attenuates the offset of that block by that gain. Therefore, the input-referred offset of the 5-bit flash can be written as:

$$\sigma\left(\mathrm{V}_{\mathrm{In-Off}}\right) = \sqrt{\mathrm{K}_1^2\sigma^2\left(\mathrm{V}_{\mathrm{Off_1}}\right) + \left(\frac{\mathrm{K}_2}{\mathrm{A}_1}\right)^2\sigma^2\left(\mathrm{V}_{\mathrm{Off_2}}\right) + \frac{1}{\left(\mathrm{A}_1 \times \mathrm{A}_2\right)^2}\sigma^2\left(\mathrm{V}_{\mathrm{Comp-Off}}\right)}, \tag{22}$$

where $\mathrm{A}_{1,2}$ are the gains of the first- and second-stage preamplifiers, and $\mathrm{K}_{1,2}$ are the averaging coefficients associated with the first- and second-stage preamplifiers, Equation 15, 18, and 21.

Since, the total input-referred offset budget of the 5-bit flash is 7.8125 mV (3σ) with 500 mV full scale, a low-offset comparator topology is essential. However, in most reported comparator topologies, the input devices of the comparator are in deep-triode region at the beginning of the latch phase, Figure 34(d). Consequently, the transconductance of the input devices are low. Thus, the input-referred offset can be substantial. However, in a tail-latched dynamic comparator, the input devices can be kept in saturation at the beginning of the latch phase. Therefore, the input-referred

offset of a tail-latched dynamic comparator can be designed to be small, [25, 59, 60]. The schematic of the comparator used in this design is given in Figure 34(c).

The input-referred offset of the comparator used in this design has a standard deviation of about 1.5 mV. Figure 35 shows the histogram of the input-referred offset of the comparator. The contributors of the input-referred offset of the 5-bit flash along with their values are tabulated in Table 8. Furthermore, the output of the comparator with a small input after a large input of same and opposite sign are given in Figure 36. The step response of the pre-amplifier block is given in Figure 37. Finally, the transient response of the 5-bit flash to a ramp input is given Figure 38.

Table 8: Simulated Offset Values of the 5-bit Flash

Offset	**Value (mV)**
Comparator	1.5
First-Stage Amplifiers	4.4
Second-Stage Amplifiers	5.7
Input-Referred	3.5 (max)

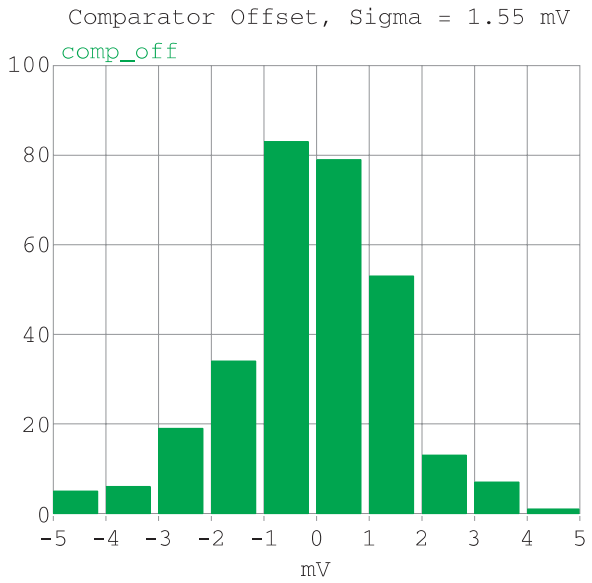


Figure 35: Simulated histogram of the comparator offset.

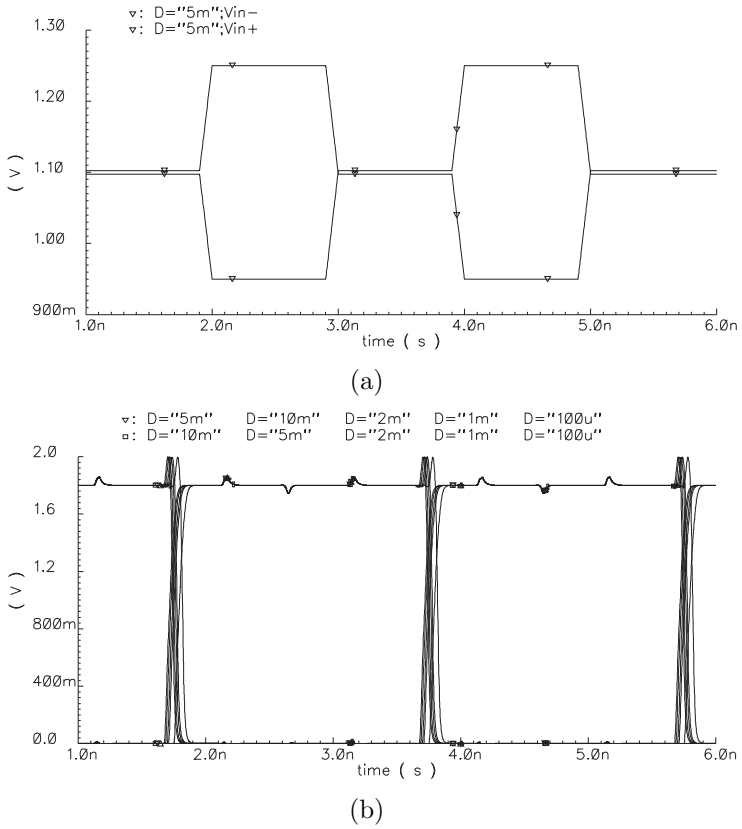


Figure 36: Transient simulation to test memory and possible reset problems in the comparator. Simulations didn't show any memory or reset problems. (a) Input waveform. (b) Output waveform.

5.2.3 5-bit Digital-to-Analog Converter

The DAC used in Stage1 is a 5-bit current-steering DAC, which must be 9-bit accurate. This DAC will be referred to as DAC1. A full unary architecture simplifies the interface between Flash1 and DAC1 as no decoding is required. Therefore, DAC1 is implemented as a full unary architecture, which consists of 30 unary cells. The schematic of a unary cell is shown in Figure 40(b). The details of the operation of a current-steering DAC will not be discussed any longer since excellent examples are reported in literature, [50, 61]. However, some of the typical design problems are discussed in the following.

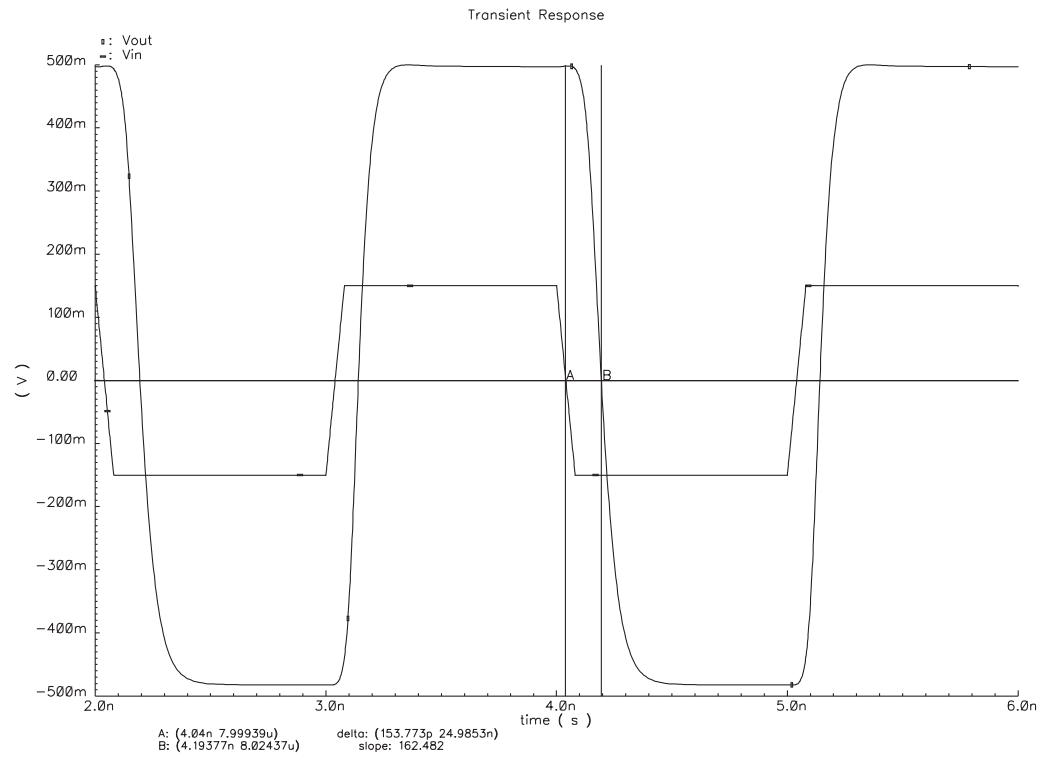


Figure 37: Step response of the preamplifier block.

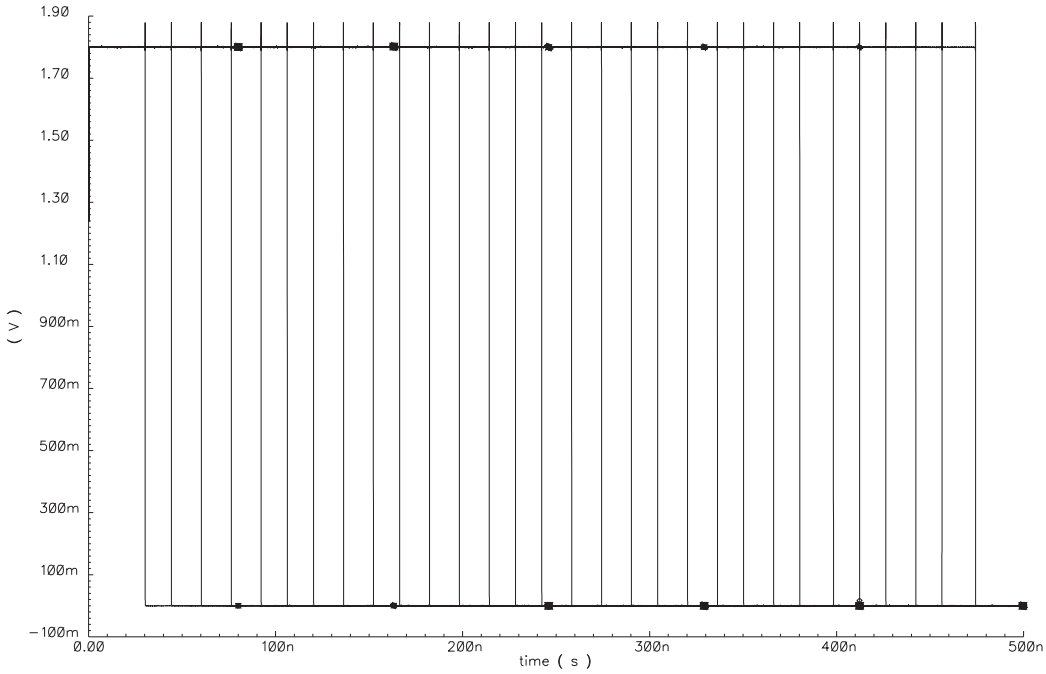


Figure 38: The transient response of the 5-bit flash to a ramp input.

Sizes of the current-source transistors of a unary cell are chosen to guarantee the matching requirements for 9-bit accuracy. The relative standard deviation of a unit current source to obtain a desired yield with a full unary architecture is given by

$$\frac{\sigma\left(\mathrm{I}\right)}{\mathrm{I}} \leq \frac{1}{2\mathrm{C}\sqrt{2^{\mathrm{N}}}}, \tag{23}$$

where C is the inverse cumulative normal distribution evaluated at $0.5(1 + \text{yield})$, and N is the resolution of the DAC, [50, 62]. Using this relative-standard-deviation requirement, the width (W) and length (L) of the unit-current-source transistors can be calculated using Equations 24 and 25, [50, 62, 63].

$$\mathrm{W}^2 = \frac{\mathrm{I}}{2\mathrm{KP}\left(\sigma\left(\frac{\Delta\mathrm{I}}{\mathrm{I}}\right)^2\right)}\left[\frac{\mathrm{A}_\beta^2}{\left(\mathrm{V_{GS}} - \mathrm{V_T}\right)_{\mathrm{CS}}^2} + \frac{4\mathrm{A}_{\mathrm{V_T}}^2}{\left(\mathrm{V_{GS}} - \mathrm{V_T}\right)_{\mathrm{CS}}^4}\right] \tag{24}$$

$$\mathrm{L}^2 = \frac{\mathrm{KP}}{2\mathrm{I}\left(\sigma\left(\frac{\Delta\mathrm{I}}{\mathrm{I}}\right)^2\right)}\left[\frac{\mathrm{A}_\beta^2}{\left(\mathrm{V_{GS}} - \mathrm{V_T}\right)_{\mathrm{CS}}^2} + \frac{4\mathrm{A}_{\mathrm{V_T}}^2}{\left(\mathrm{V_{GS}} - \mathrm{V_T}\right)_{\mathrm{CS}}^4}\right] \tag{25}$$

The statistical mismatch values can be optimized by sizing the unit-current-source transistors according to the values given in Equations 24 and 25. However, systematic mismatch can only be reduced by utilizing proper layout practices such as common-centroid topologies and interdigitating [64]. The unit-current-source transistors 1 to 30 are laid out in a common-centroid scheme with appropriate dummy transistors according to the floor plan shown in Figure 39.

The output of a current-steering DAC may exhibit significant transients caused by switching, [50, 61]. These transients are commonly referred to as output glitch.

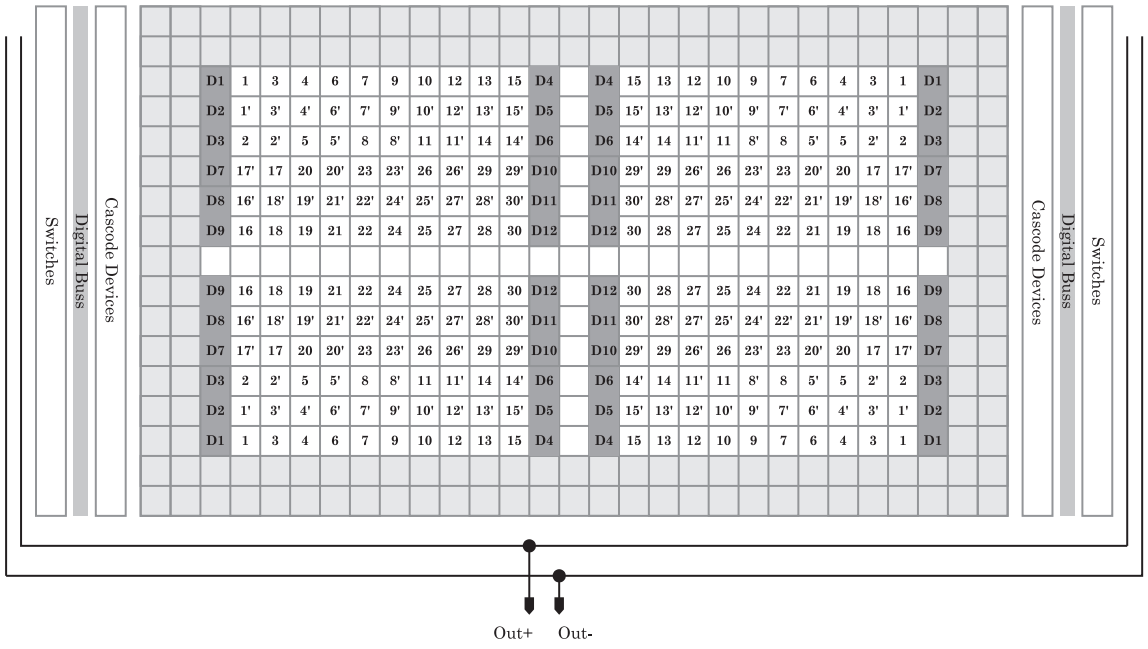


Figure 39: Common-centroid layout of the unit-current sources of DAC1.

The coupling from the control signals that steer the unit current source, causes asymmetrical gate currents because the values of the gate-to-source capacitors of the two switch transistors within a unit cell are not identical. Typically, the rise and fall times of the controlling signals are also not very well controlled. These factors result in transients in the unit current. These transients occur at every clock edge and result in differential-mode as well as common-mode transients at the output, Figure 40(c).

Another source of the output glitches is the coupling from the controlling signals (D+ and D−) that disturbs the gate voltages of the current-source transistors. The source voltage of the current-steering switches dips at each edge of the controlling signals, see Figure 40(d). The transient common-source voltage (dip) couples to the gate of the cascode transistor and eventually to the gate of the current-source transistor. This coupling has a similar effect as the first one: It changes the unit

current and results in both differential- and common-mode variations at the output. The transients stemming from unequal gate currents can be reduced by making the rise and fall times of the controlling signals as close to each other as possible. Also, using small switch devices reduces the output glitches. Moreover, connecting by-pass capacitors to the gates of the transistors that comprise the tail-current source, reduces the transients caused by the voltage dip on the common-source node.

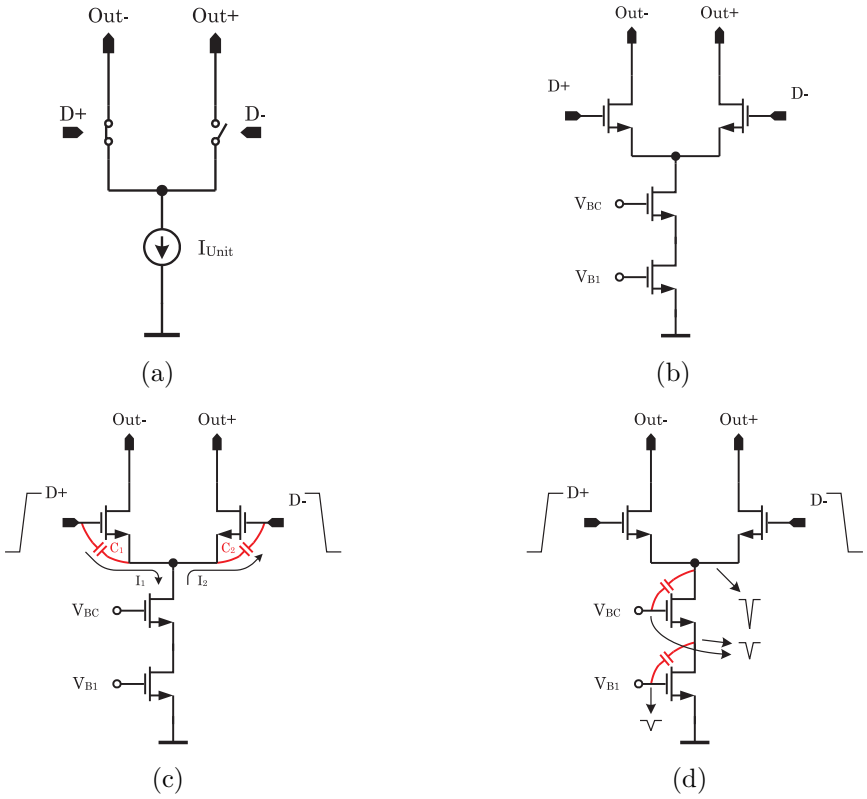


Figure 40: Current-steering cell. (a) Ideal implementation. (b) NMOS implementation. (c) Unequal gate currents caused by unsymmetrical coupling and difference in gate-to-source capacitors. (d) Disturbance on the gates of the unit-current-source transistors due to the parasitic coupling from the common-source node.

The reference current for DAC1 is generated by forcing the reference voltage across a poly resistor. The schematic of the circuit that generates the reference current is shown in Figure 41. Note that, the nodes VBC and VB1 shown in Figure 41 drive

the nodes with the same names in Figure 40.

The LSB voltage of DAC1 is given by:

$$\mathrm{DAC_{LSB}} = \frac{\mathrm{V_{REF}}}{\mathrm{R_{REF}}} \times \mathrm{R_{L-MSSA}} + \mathrm{I_{Trim}} \times \mathrm{R_{L-MSSA}} \tag{26}$$

where, $\mathrm{V_{REF}}$ is the reference voltage, $\mathrm{R_{REF}}$ is the resistance across which the reference voltage is forced (see Figure 41), $\mathrm{R_{L-MSSA}}$ is the load resistance that converts the current output of DAC1 into voltage, and $\mathrm{I_{Trim}}$ is the trim current. Note that, $\mathrm{R_{L-MSSA}}$ is the load resistor of the residue generator block shown in Figure 32. Furthermore, the gain of DAC1 is dependent on resistor ratios. Therefore, it is more immune to PVT changes. The gain error associated with DAC1 can be trimmed out by a trim current, which changes the value of the unit current of DAC1. A trim pin is assigned for the trim current to be able to change the DAC1 gain externally.

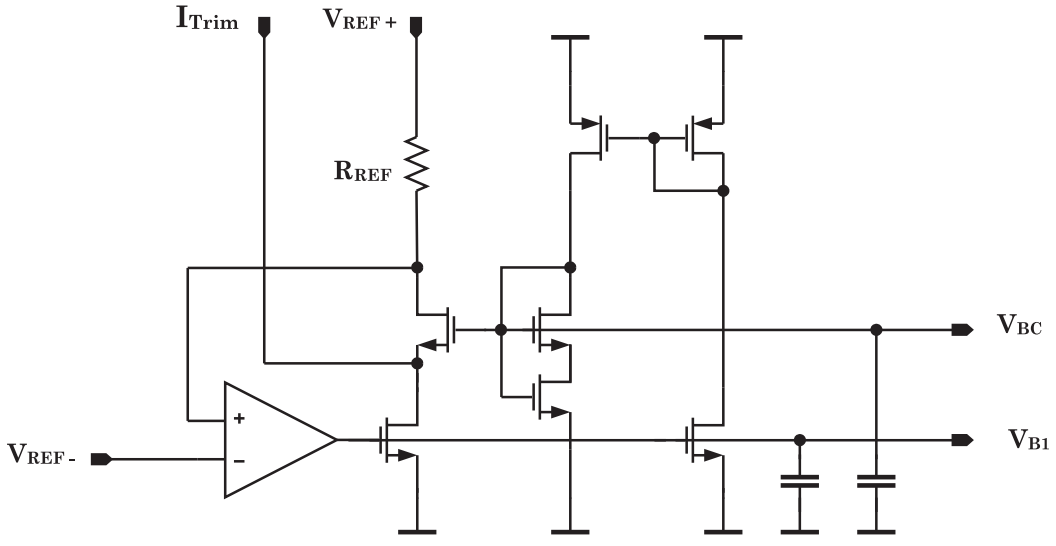
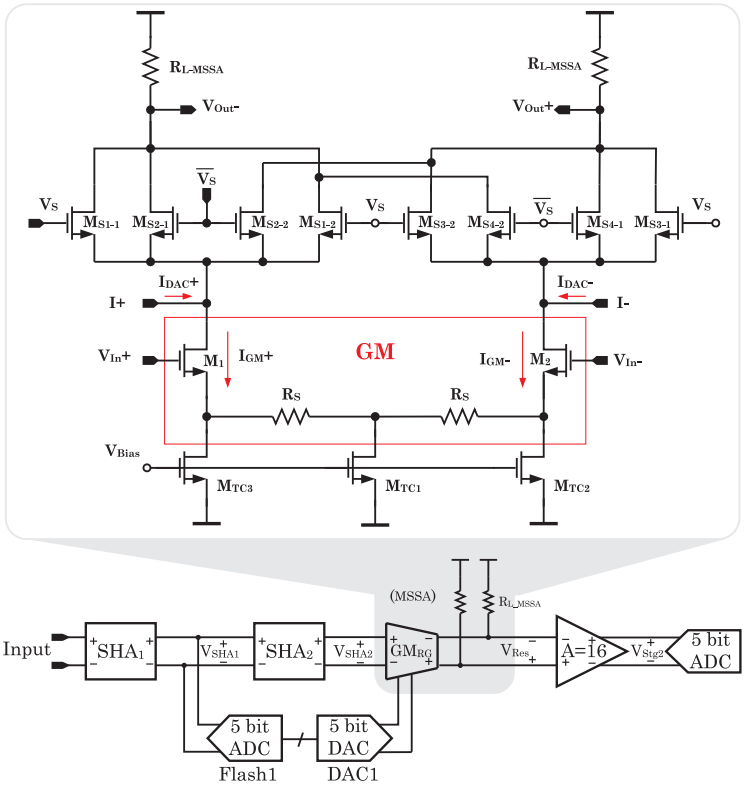


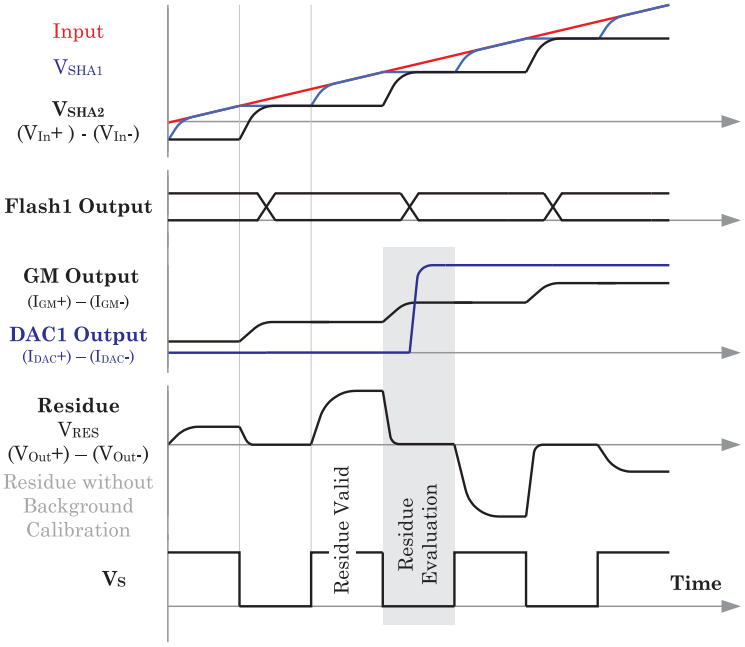
Figure 41: Schematic of the reference-current generator.

5.2.4 Residue Generation

The main objective of this design is to use local feedback to achieve high-conversion speed. Therefore, the residue is not generated by an accurate global-feedback amplifier as in the case of all switched-capacitor designs. In this design, the residue is generated in the current domain by a block, which will be referred to as mode-switching summing-amplifier (MSSA). The schematic of the MSSA is given in Figure 42(a). The MSSA has a differential voltage input ($V_{In}+, V_{In}-$) and a differential current input (I+, I−). DAC1, which generates a current output, drives the current input of the MSSA. The voltage input of the MSSA, however, is driven by SHA_2. Note that, the output of SHA_2 is an accurate discrete replica of the input, see Figure 42(b). The MSSA simply converts its voltage input into current by a source-degenerated differential pair, which is denoted by GM in Figure 42(b), and subtracts its current input from this current. Thereby, the MSSA generates the residue. The topology of the MSSA is similar to the topology of the SHAs. The only significant difference is in the switching scheme. In the MSSA, the switches are organized such that they switch the MSSA from differential mode to common mode. However, in the SHAs the switches are organized such that the output current is steered to the actual or dummy loads.



(a)



(b)

Figure 42: Mode-Switching Summing Amplifier. (a) Schematic. (b) Input, SHA outputs, DAC1 output, signals within MSSA, and residue signal.

The output of the MSSA does not represent a valid residue when SHA_2 is in the track mode, see Figure 42(b). When the output is not a valid residue, the MSSA is switched to common-mode, which prevents Stage2 from overloading. Note that, the current produced by DAC1 is subtracted from the current generated by the source-degenerated input differential pair before the current-steering switches, see Figure 42(a). Also, since the MSSA operates in common-mode when the residue is not valid, the output of the MSSA starts from the same initial condition as it is switched to differential-mode operation. This operation is analogous to resetting the amplifier in a switched-capacitor MDAC. Therefore, it eliminates the memory effects. The residue waveform during sample and amplify phases along with other relevant signal are shown Figure 42(b).

Since the SHAs and the MSSA have similar topologies, their clocking scheme is also similar. Like the clocks used in the SHAs, the clock signals used in the MSSA have certain common-mode levels and swings, which keep the switch transistors in saturation when they are on. The clock signals keep the input differential pair also in saturation during normal operation conditions.

5.2.5 Interstage Amplifier

The interstage amplifier consists of two stages. Each stage is a resistively-loaded cascode differential amplifier with buffered outputs. The buffers are simple source followers, which improve step response and provide level shifting between the stages. A simplified schematic of the interstage amplifier is given in Figure 43. Nominally, each stage has a gain of 4. If source degeneration is used in the input differential

pair to improve linearity, the effective transconductance reduces. Therefore, larger load resistors must be used to get the desired gain of 4. On the other hand, using larger load resistors reduce the BW. Therefore, the step response, and conversion speed limits are degraded. Consequently, the differential pairs used in the interstage amplifier are not source degenerated. Note that, this has an adverse effect on linearity and gain variation. Nonetheless, since the amplitude of the signal (the residue) at the input of the interstage amplifier is small, the inherent linearity of the differential pair is sufficient for this design. The third harmonic distortion of a MOSFET differential pair is given by

$$\mathrm{HD3} = \frac{1}{32}\left(\frac{\mathrm{V_d}}{\mathrm{V_{od}}}\right)^2, \tag{27}$$

where $\mathrm{V_d}$ is the differential input voltage and $\mathrm{V_{od}}$ is the overdrive voltage of the differential pair. With 150 mV overdrive and 64 mV differential voltage, the third harmonic distortion of a differential pair is

$$\mathrm{HD3} = \frac{1}{32}\left(\frac{64}{150}\right)^2 = 5.7 \times 10^{-3}, \tag{28}$$

which is better than 5-bit linearity.

The sensitivity of the interstage gain to several circuit parameters is given by

$$\begin{aligned}\frac{\sigma^2(\Delta \mathrm{A})}{\mathrm{A}^2} = 2\Bigg[&\frac{\sigma^2(\Delta \mathrm{R_L})}{\mathrm{R_L^2}} + \sigma^2(\Delta \mathrm{gm_1})\mathrm{R_L^2} \\ &+ \frac{\sigma^2(\Delta \mathrm{gm_2})\mathrm{gmb_2^2}}{(\mathrm{gm_2}+\mathrm{gmb_2})^2\mathrm{gm_2^2}} + \frac{\sigma^2(\Delta \mathrm{gmb_2})}{(\mathrm{gm_2}+\mathrm{gmb_2})^2}\Bigg],\end{aligned} \tag{29}$$

where $\mathrm{R_L}$ is the load resistance, gm1 is the input transconductance, gm2 is the buffer

transconductance, and gmb_2 is the back-gate transconductance of the buffer. The gain variations in the interstage amplifier is not sufficient for the design. Therefore, a background calibration technique is utilized to compensate the gain variations and make the design immune to gross interstage gain errors. This calibration technique is explained in the following section.

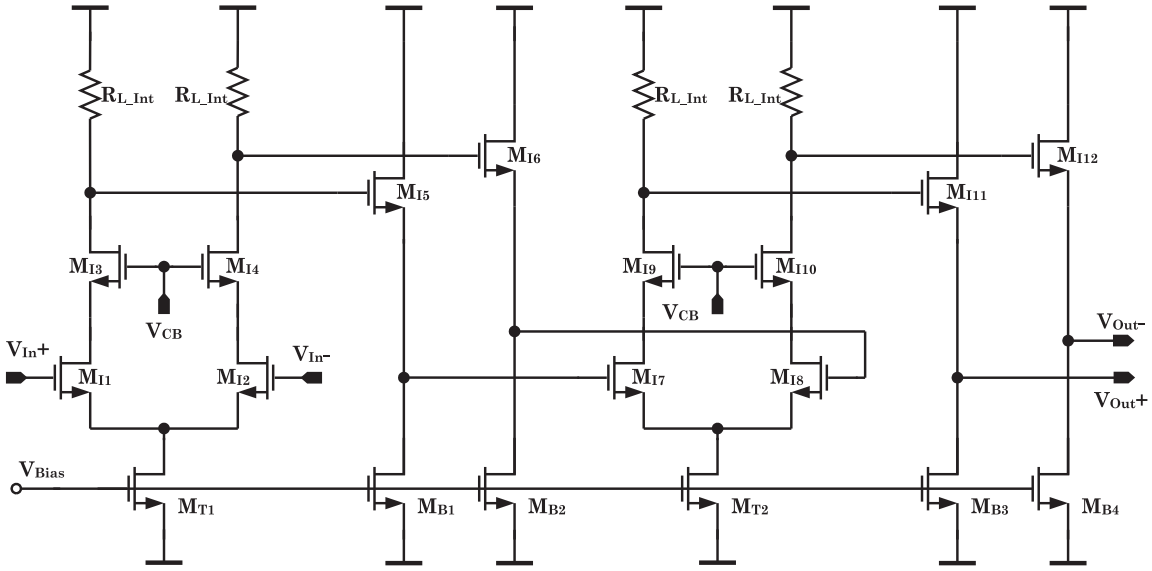


Figure 43: Schematic of the interstage amplifier.

5.2.6 Reference Voltage Generation

As discussed in the previous section, the proposed ADC architecture utilizes an open-loop residue amplifier with a gain of 16. As shown in Table 7, the residue amplifier has to be only 5-bit accurate. The linearity of the residue amplifier is sufficient for the design with only 150 mV overdrive, as predicted by Equation 28. However, the gain accuracy across PVT variations is not sufficient. The gain variations in the residue amplifier are compensated by the proposed background calibration. This calibration method relies on scaling the reference of Stage2 with the same factor that alters the

gain of the interstage amplifier from its ideal value. Therefore, the reference of Stage2 tracks the changes in the interstage gain and the interstage gain variations do not affect the operation of the ADC. However, as the interstage gain changes, the offset requirement of Flash2 changes as the full-scale value of Stage2 changes. A rigorous description of the calibration method is presented in the following.

The input signal of the ADC can be reconstructed from the digital outputs of Stage1 and Stage2, and quantization error as:

$$\begin{aligned} V_{In-reconst} &= D_1 \frac{V_{REF}}{2^5} + D_2 \frac{1}{G_1} \frac{V_{REF}}{2^5} + V_Q \\ &= V_{In}, \end{aligned} \tag{30}$$

where $V_{In-reconst}$ is the reconstructed input signal, V_{REF} is the reference voltage, D_i is the digital output of Stage$i$, G_1 is the (ideal) gain of Stage1, and V_Q is the quantization error. If, for some reason, the gain of the interstage amplifier drifts by ϵ, the reconstructed input signal becomes:

$$\begin{aligned} V_{In-reconst} &= D_1 \frac{V_{REF}}{2^5} + D_2 \frac{1}{\epsilon \times G_1} \frac{V_{REF}}{2^5} + V_Q \\ &\neq V_{In}. \end{aligned} \tag{31}$$

The interstage gain error can be compensated by scaling the reference of Stage2 with the same factor, ϵ. In this case, the reconstructed input signal boils down to the ideal case as shown in Equation 32.

$$
\begin{aligned}
V_{In-reconst} &= D_1 \frac{V_{REF}}{2^5} + D_2 \frac{1}{\epsilon \times G_1} \frac{\epsilon \times V_{REF}}{2^5} + V_Q \\
&= D_1 \frac{V_{REF}}{2^5} + D_2 \frac{1}{G_1} \frac{V_{REF}}{2^5} + V_Q \\
&= V_{In}
\end{aligned} \tag{32}
$$

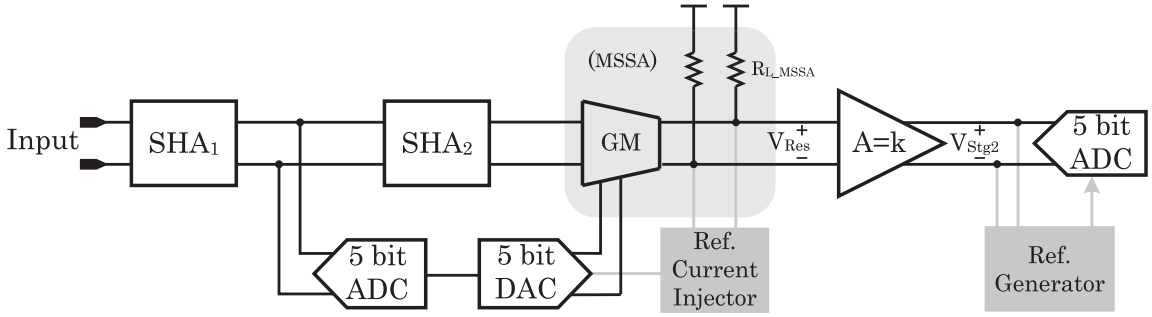


Figure 44: Block diagram of the ADC with the calibration blocks.

As explained earlier, the MSSA operates in common mode and does not generate a differential output during half of the clock period. Therefore, the interstage amplifier is not used for residue amplification during this phase. Instead, the interstage amplifier is used to generate the reference for Stage2. This is done as follows:

- During the common-mode operation phase of the MSSA, a calibration current, I_{Cal} is injected to the output nodes of the MSSA.
- The calibration current generates a differential voltage at the output of the MSSA.
- The differential voltage is amplified by the interstage amplifier.
- The output of the interstage amplifier is sampled at the end of the common-mode operation phase. This sampled voltage, $V_{Ref-Gen}$, can be simply written as:

$$V_{Ref-Gen} = I_{Cal} \times R_{L-MSSA} \times A_{Int}, \tag{33}$$

where A_{Int} is the gain of the interstage amplifier. Also, if the calibration current I_{Cal} is chosen to be a scaled replica of the reference current used in DAC1, $V_{Ref-Gen}$ becomes:

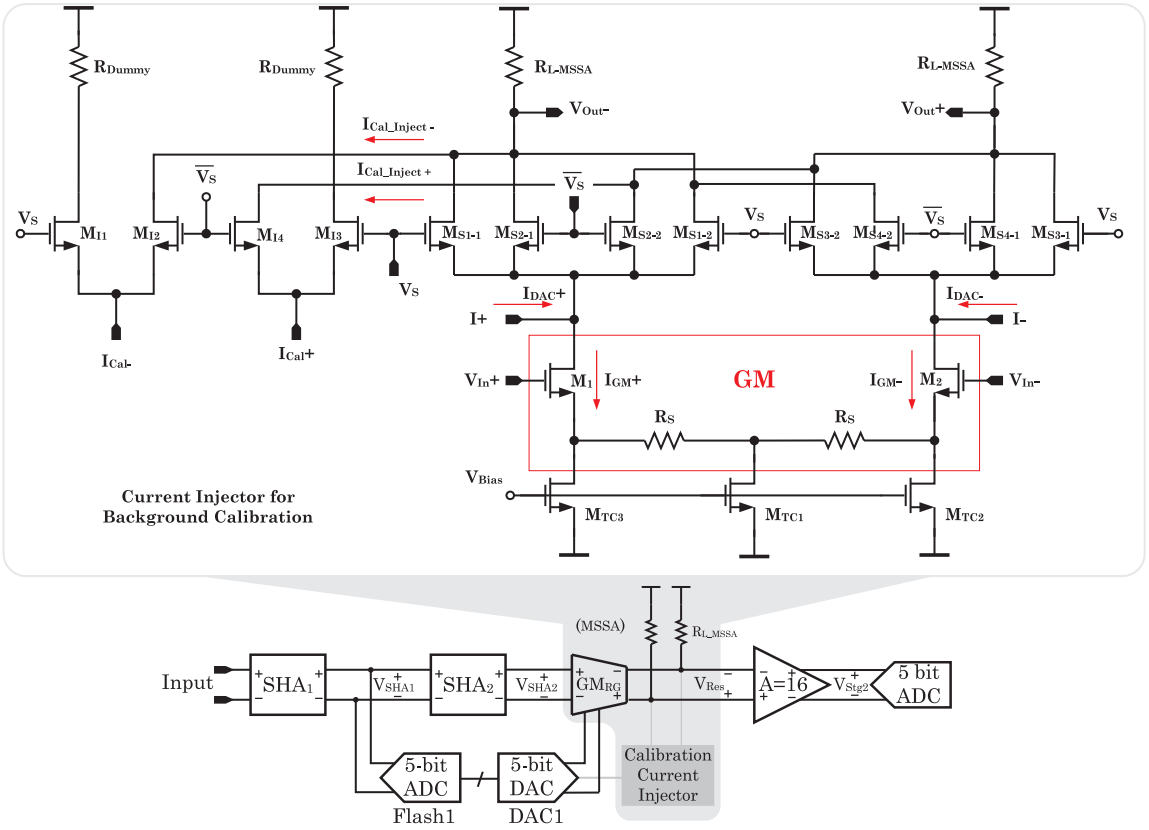
$$V_{Ref-Gen} = \alpha \left[\left(\frac{V_{REF}}{R_{REF}} + I_{Trim} \right) \times R_{L-MSSA} \right] \times A_{Int}, \tag{34}$$

where, α is a scaling factor, which is chosen to be 0.5 in this design for linearity purposes. The term inside the square brackets correspond to 1 LSB of Stage1. In other words, it is the step in the residue voltage, when DAC1 input changes by one code, see Equation 26. Therefore, $V_{Ref-Gen}$ is α times the reference of Stage1, if A_{Int} is at its ideal value, which is 16 in this design. Consequently, $V_{Ref-Gen}$ can be used as the reference of Stage2 after proper filtering and scaling by $1/\alpha$. If the gain of the interstage amplifier changes by any reason, $V_{Ref-Gen}$ changes by the same factor. That means, the reference of Stage2 tracks the drift in the interstage gain. Therefore, the interstage gain error is compensated as shown by Equation 32.

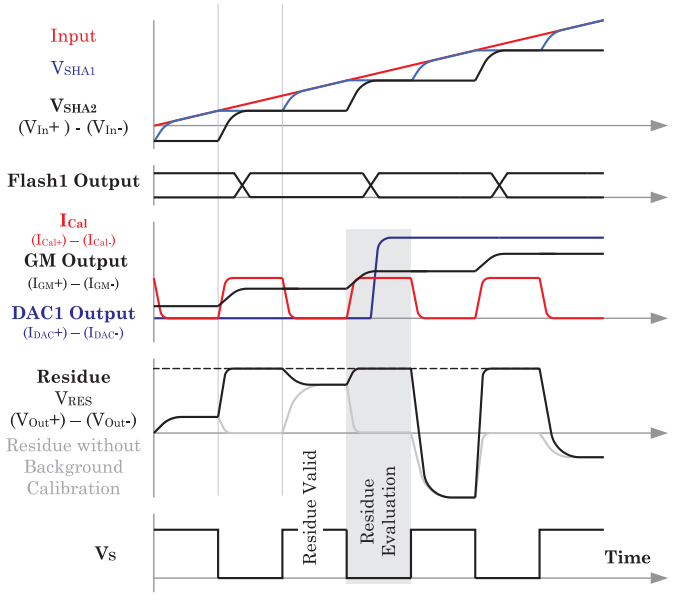
The block diagram of the ADC with the blocks necessary for the background calibration is shown in Figure 44. The calibration current is injected by a block which will be referred to as the calibration-current injector. The circuit, which samples the output of the interstage amplifier will be referred to as the reference-generator circuit. The reference-generator circuit not only samples the output of the interstage amplifier, it also filters the sampled voltage to remove the sampling glitches. The scaling factor

α in Equation 34 has to be compensated for proper operation. This is done with an off chip amplifier for debugging purposes.

A simplified schematic of the MSSA with the calibration-current injector is shown in Figure 45(a). The residue voltage, V_{Res}, along with the relevant signals in Stage1 are shown in Figure 45(b). Furthermore, reference-generator circuit, V_{Res}, and the clocking scheme for the reference-generator circuit are shown in Figures 46(a) and 46(b) respectively. The reference-voltage generator samples the same signal level every time, see Figure 46(b). Therefore, its acquire BW is not critical. Accurate settling can be achieved in several clock cycles.



(a)



(b)

Figure 45: Mode switching summing amplifier. (a) Schematic. (b) Various signals within Stage1 and MSSA, and the residue.

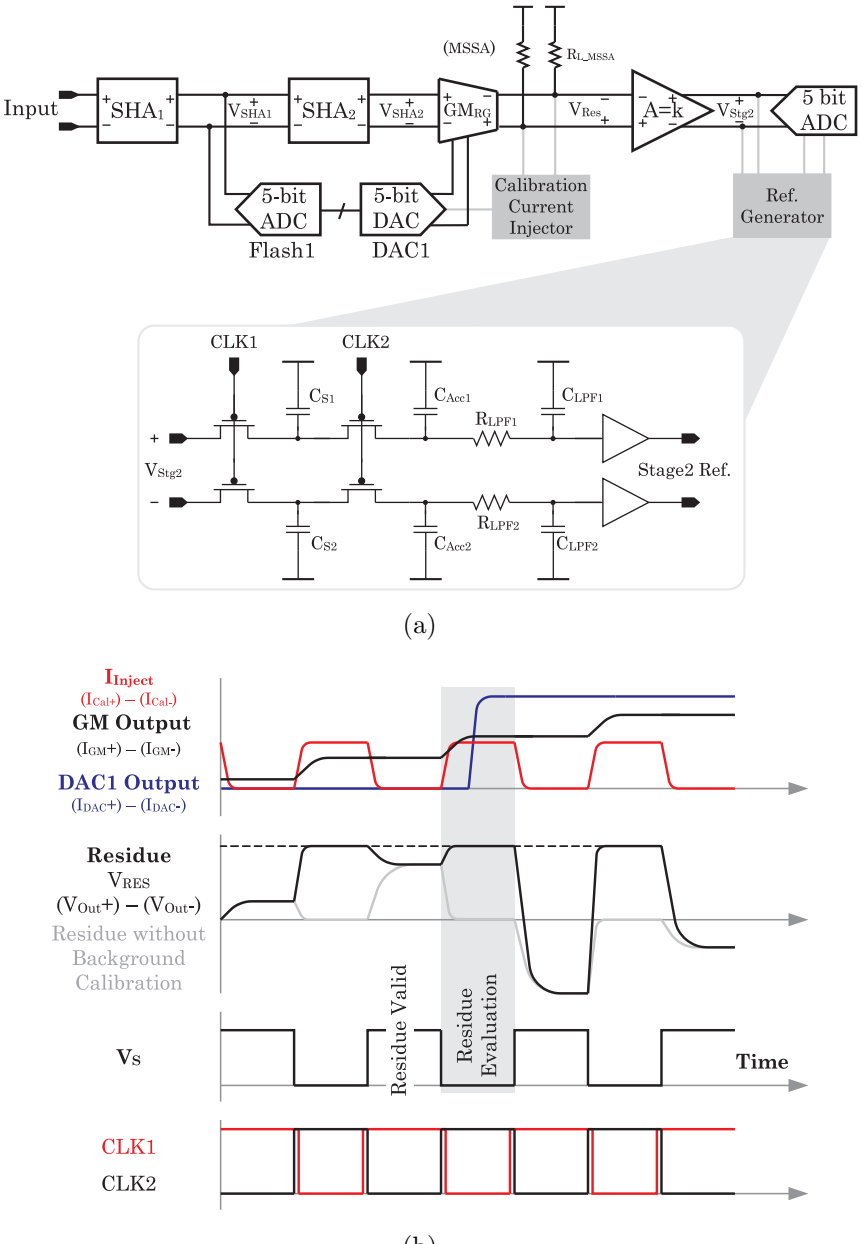


Figure 46: Reference voltage generator. (a) Schematic. (b) Various, signals within MSSA, residue, and clocking scheme.

5.2.6.1 Compensation of the Interstage Gain Nonlinearity

The proposed calibration method can be utilized to correct the nonlinearity of the interstage amplifier as well. In this case, the transfer function of the interstage amplifier can be approximated in a piece-wise-linear fashion. Therefore, the current injector has to inject multiple current levels. Thereby, the reference-generator circuit can sample the output of the interstage amplifier at different output levels. The transfer function of the interstage amplifier can be approximated as a linear summation of the samples corresponding to different values of the output of the interstage amplifier. For example, in the most simplistic case, the injected current can have two levels. One level can be chosen to force V_{Stg2} to be 3/8 of the full scale. The second level can be chosen to force V_{Stg2} to be 1/2 of the full scale. These two current levels may be injected at alternating periods or their injection order can be randomized. Even though, randomizing the order of the injection complicates the switching networks, it spreads the tones that can be generated by the switching activity into the noise floor. Note that, since the injected current has 2 levels, V_{Stg2} corresponding to each current level has to be sampled and accumulated by a separate switched-capacitor network. The reference for Stage2 can be generated as a linear summation of the output of these 2 networks. Figure 47 depicts a simplified nonlinearity correction scheme.

With nonlinearity correction, the overall resolution of the converter can be improved. Also, since a larger nonlinearity can be tolerated in the interstage amplifier, the resolution of Stage1 can be reduced to a more optimum level for lower power consumption and noise. However, the nonlinearity correction scheme is not attempted in this design.

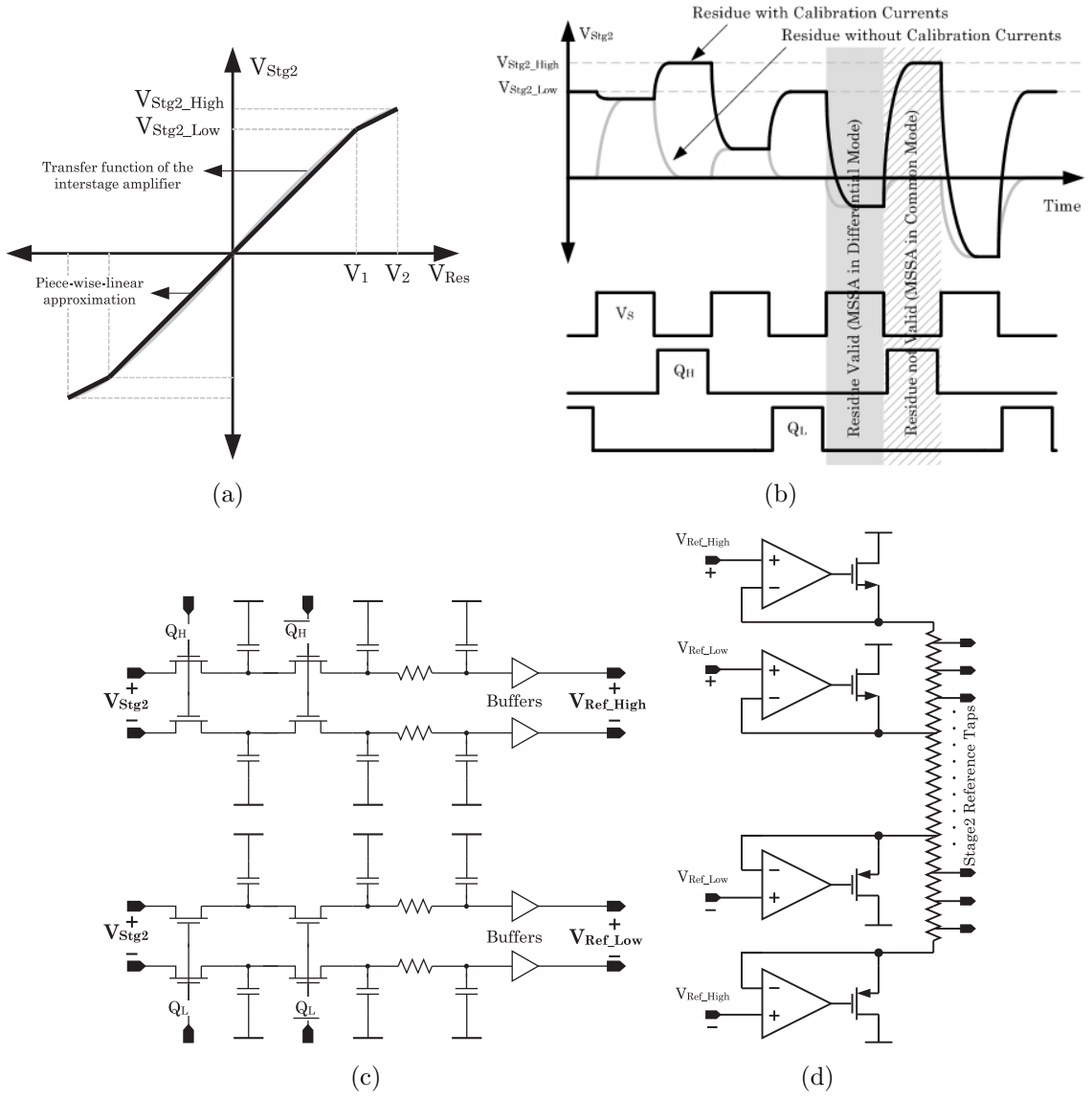


Figure 47: Nonlinearity compensation. (a) Transfer function of the interstage amplifier. (b) Residue. (c) Reference generator. (d) Reference buffer.

5.2.7 Digital Circuitry

All of the digital gates used in this design are custom designed. The D flip-flops are implemented with true-single-phase clock topology, [65]. The D flip-flops used in the clock generation block are functional at clock rates higher than 4 GHz. The D flip-flops used in the ADC chip are same as the ones used in the SHA chips. The SHA chip can achieve sample rates as high as 1.5 GHz with 10 bit accuracy. Since the external clock frequency is divided by 2 to obtain 50 % duty cycle regardless of the common-mode level of the clock, the D flip-flops are designed to operate at frequencies higher than 4 GHz. The D flip-flops are designed faster than they need to be to investigate the behavior of the SHA chip at high sample rates. The thermometric to binary encoder for DAC1 is implemented as a read-only memory. The adders used in the error correction and output formatting block are realized with a CMOS topology.

5.3 Alternative Calibration Methods

The calibration proposed in this research is done in an analog fashion by scaling the back-end reference to compensate the variations in the interstage gain. Therefore, the digital reconstructor could use the ideal gain of the interstage amplifier. The ADC's output was reconstructed from the Stage1 and Stage2 bits using the following equation.

$$D_{Out} = A_{Ideal}D_{Stg1} + D_{Stg2} = 16 \times D_{Stg1} + D_{Stg2} \tag{35}$$

where D_{Out} is the digital output of the entire ADC, D_{Stgi} is the digital output of the i^{th} stage, and A_{Ideal} is the ideal gain of the interstage amplifier. In this design the

ideal gain of the interstage amplifier was 16.

If the proposed calibration method is realized in the digital domain, Stage1 and Stage2 can use the same reference. The digital estimate of the interstage gain can be obtained by converting the output of the reference-generator block into digital by an accurate but slow ADC. In this case, the digital reconstruction must use the estimated gain of the interstage amplifier as opposed to its ideal gain as shown in Equation 36.

$$D_{Out} = A_{Est} D_{Stg1} + D_{Stg2} \tag{36}$$

where A_{Est} is the estimated gain of the interstage amplifier.

The digital version of the proposed calibration method is shown in Figure 48. Note that, Stage2 (back-end) can digitize the injected calibration signal with some modifications, [27, 66]. The nonlinear calibration mentioned earlier can be implemented in the digital domain in a similar fashion.

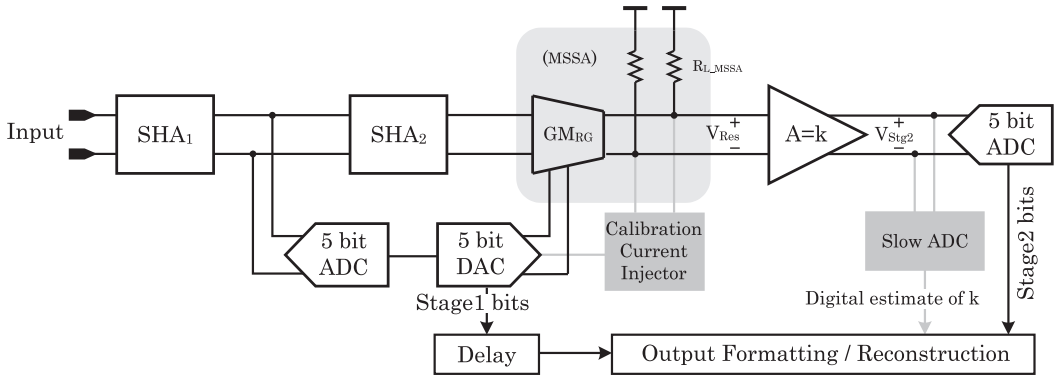


Figure 48: Digital implementation of the proposed calibration method. Both stages use the same reference. However, the interstage gain error is compensated in the digital domain during output reconstruction.

Several other calibration techniques are reported in literature [27, 39, 42, 66]. The

calibration technique reported in [27] relies on injecting a random signal (dither) at the input of the MDAC during amplify phase and estimating the interstage gain by auto-correlating this dither to the back-end bits in the digital domain. The block diagram of the dither-based calibration is shown in Figure 49. Using the update equation given by 37, the correlation engine iteratively drives the term inside the square brackets to zero and the closed-loop gain of the MDAC is estimated, which is A_{Est}. As in the previous case, the estimated closed-loop gain is used during digital reconstruction as shown in Equation 36.

The update equation for the correlation engine can be:

$$A_{Est}[n+1] = A_{Est}[n] - \mu RN[n]\Big[A_{Est}[n]RN[n] - D_{Back-end}[n]\Big] \tag{37}$$

where $A_{Est}[n+1]$ is the next estimate of gain, $A_{Est}[n]$ is the current estimate of gain, μ is a constant, and RN[n] is the current value of the random number generated by the random-number generator.

Since this method relies on estimating the closed-loop gain of MDAC1, the gain estimation must be at least as accurate as the ADC itself. Further, this method not only compensates the interstage errors but also the reference and settling errors. A nonlinear version of this calibration was demonstrated as well, [39].

The calibration reported in [66] depends on estimating the open-loop gain of the amplifier used in MDAC1. The block diagram of this calibration method is shown in Figure 50. In this method, the input of MDAC1's amplifier is sampled by a fast SHA and digitized by a slow ADC. The LMS algorithm uses this slow ADC's output (Digitized value of the input of MDAC1's amplifier - e) and the back-end bits

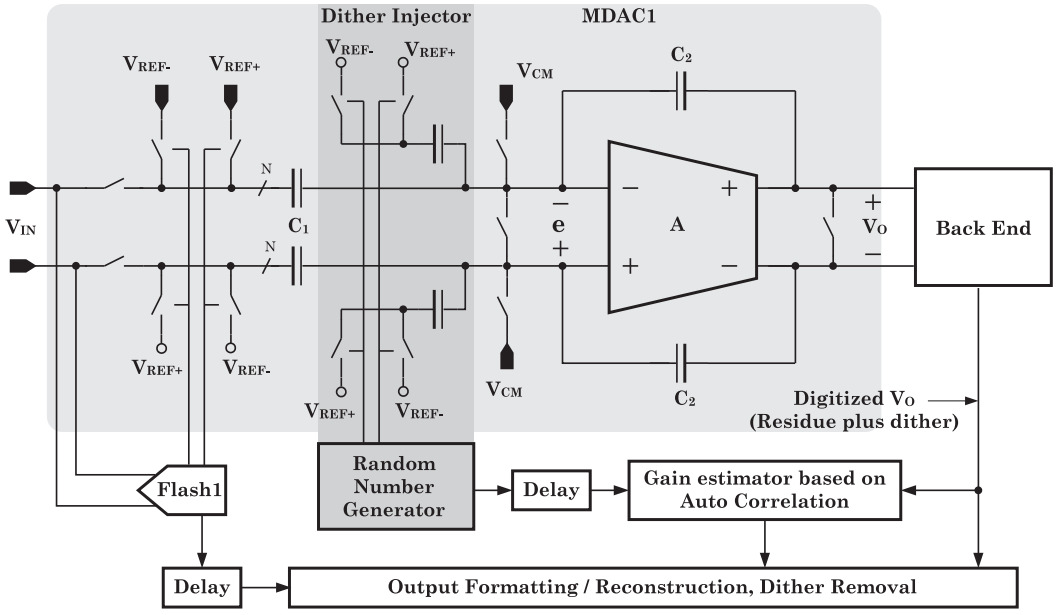


Figure 49: Dither-based calibration. The interstage gain error is compensated by estimating the interstage gain error by injecting a random dither in the MDAC. The interstage error is estimated by auto-correlating the injected dither to the back-end ADC output.

(digitized value of the output of MDAC1's amplifier) to estimate the open-loop gain of MDAC1's amplifier. An update equation similar to 37 can be used. Further, it can be shown that the ideal value of MDAC1's output is given by:

$$V_{O-Ideal} = V_O + \frac{C_1}{C_2}\frac{V_O}{a_{Est}} \tag{38}$$

where $V_{O-Ideal}$ is the output of MDAC1 with an infinite-open-loop-gain amplifier, V_O is the output of MDAC1, C_1 is the input capacitor, C_2 is the feedback capacitor, and a_{Est} is the estimated open-loop gain of the MDAC1's amplifier.

The digital reconstructor must correct the back-end bits before they are appended to Stage1 bits because the back-end digitizes the non-ideal value of MDAC1 output.

The correction applied to the back-end bits is essentially the digital version of Equation 38. The correction applied to the back-end bits and the reconstruction of the entire ADC bits are shown by Equations 39 and 40. Since this method relies on estimating the open-loop gain of MDAC1's amplifier, the sensitivity of the calibration to estimation accuracy is relaxed, [66]. Moreover, the gain estimation can be a linear or nonlinear estimation. That means, this method can also be used to correct amplifier nonlinearity as well as settling errors.

$$D_{Back-End-Ideal} = D_{Back-End} + \frac{C_1}{C_2}\frac{D_{Back-End}}{a_{Est}} \tag{39}$$

$$D_{Out} = \frac{C_1}{C_2}D_{Stage1} + D_{Back-End-Ideal} \tag{40}$$

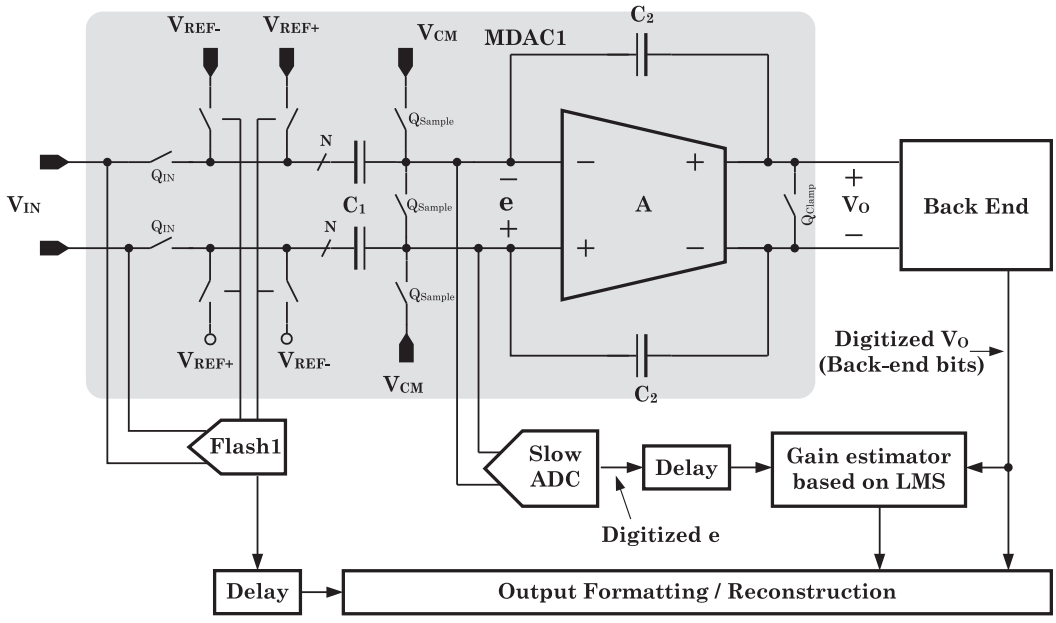


Figure 50: The calibration method that relies on estimating the open-loop gain of the MDAC amplifier.

5.4 Simulation Results

Several critical simulation results are provided in this section. Simulated residue signal is shown in Figure 51. Note that the calibration was disabled during this simulation to show the residue in detail. The ADC was simulated with different sampling frequencies, the input voltage was reconstructed from Flash1 bits and the residue, and the linearity of this reconstructed signal was investigated. The spectrum of the reconstructed signal at 700 MHz sampling frequency is given in Figure 52. The harmonics of the reconstructed signal versus the sampling frequency is shown in Figure 53.

The spectra of the reconstructed input signal before and after the calibration loop had converged are shown Figure 54. A simulation that shows the convergence of the output of the reference-generation circuit is shown in Figure 55. The output of the reference-generation circuit converges in a few μs at 700 MHz sampling frequency.

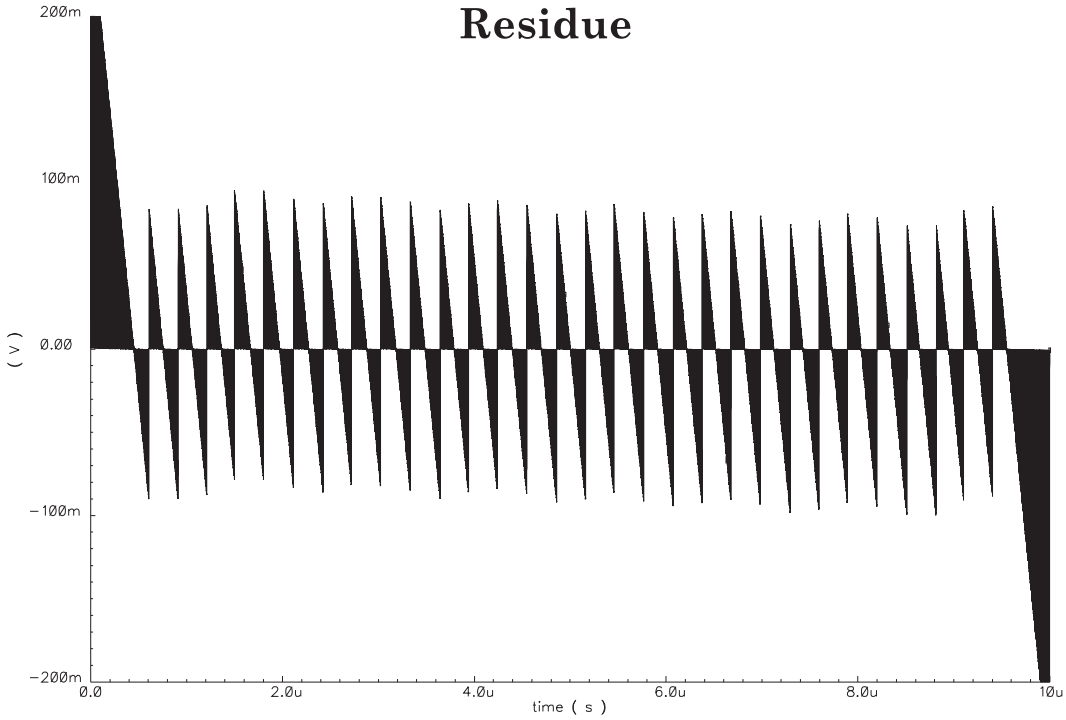


Figure 51: Residue generated after the first stage. The reference voltage was 250 mV. In this simulation, the interstage gain was less than its ideal value of 16.

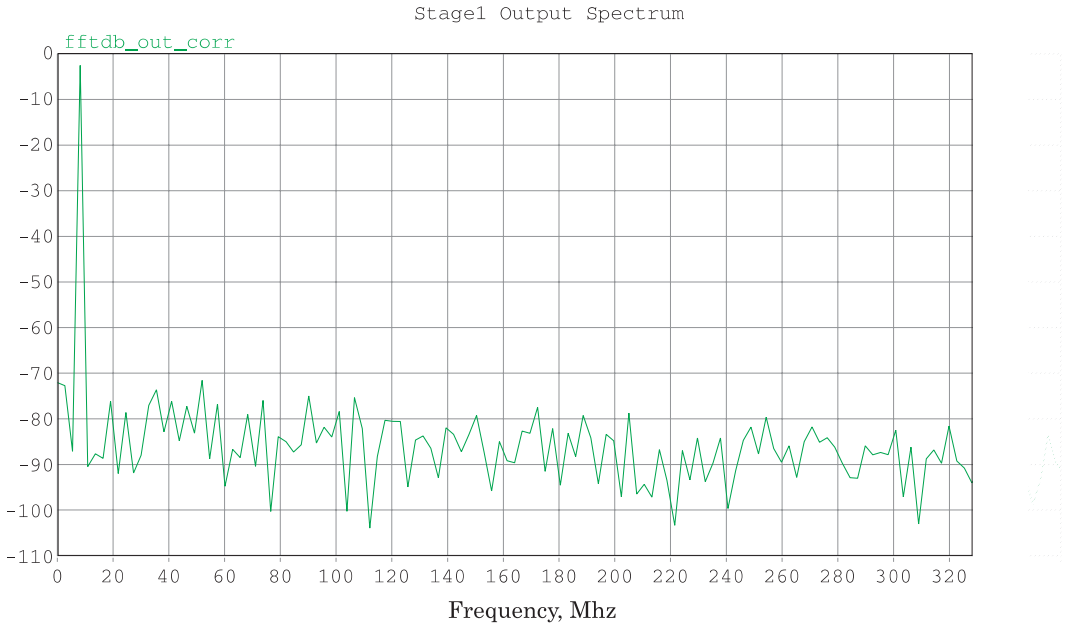


Figure 52: Spectrum of the reconstructed input voltage at 700 MHz sampling frequency.

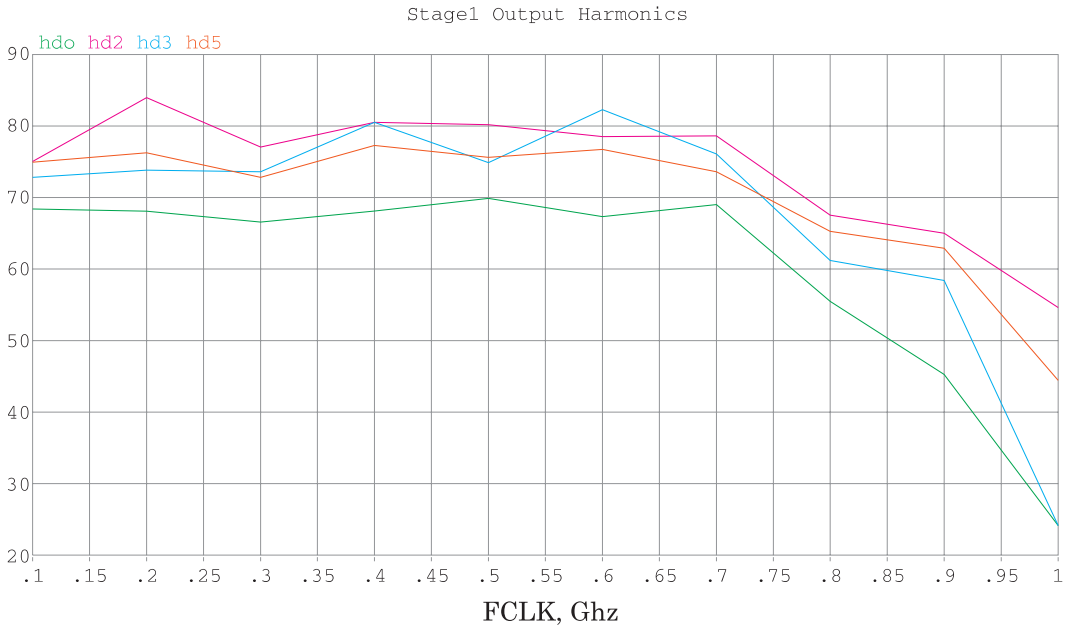


Figure 53: Spectrum of the reconstructed input voltage versus sampling frequency.

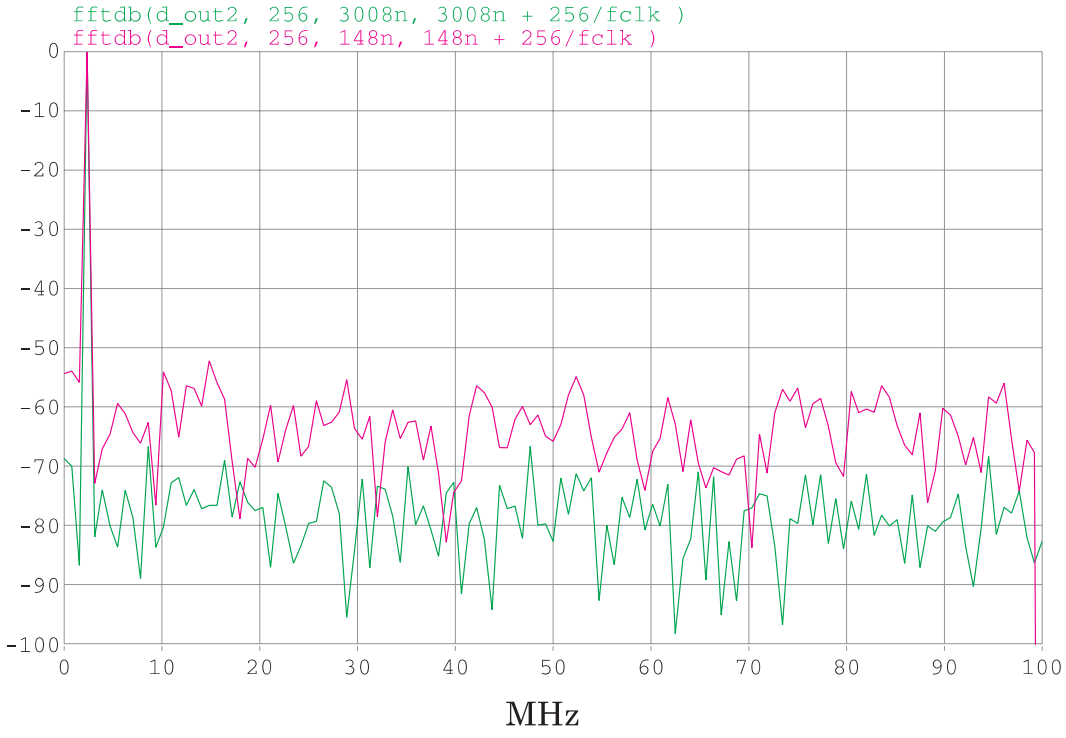


Figure 54: Spectrum of the reconstructed input voltage with and without calibration.

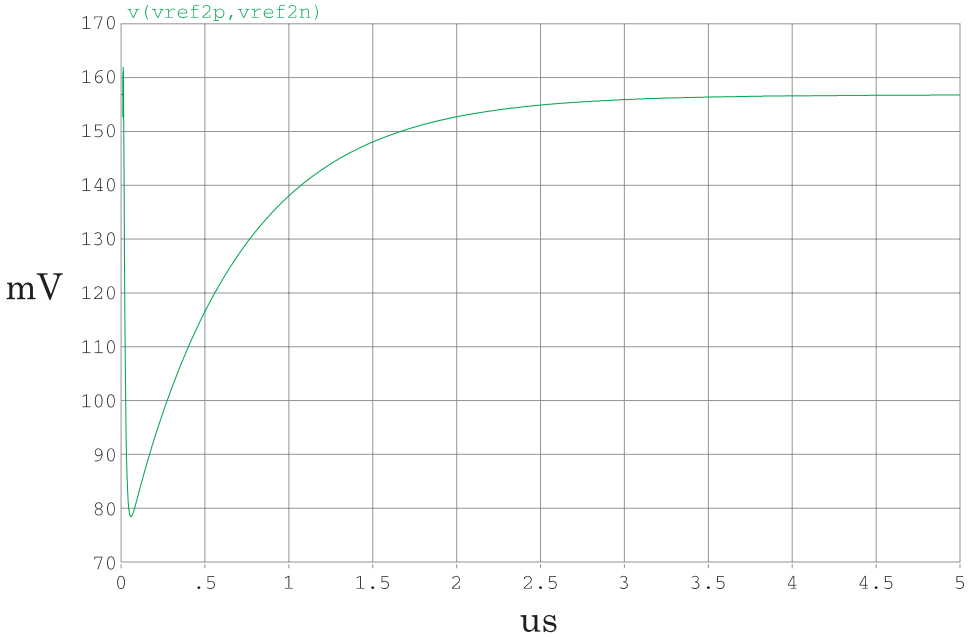


Figure 55: Convergence of the output of the reference-generation circuit.

5.5 Measurement Results

The block diagram of the test setup is shown in Figure 56. The ADC has differential analog and clock inputs. The single ended generator outputs are converted to differential signals by transformers. The analog input was band-pass filtered to clean the harmonics of the output of the signal generator. The photograph of the ADC die is shown in Figure 57. The photograph of the PCB used to test the ADC is shown in Figure 58. Finally, the schematic of this PCB is shown in Figure 59.

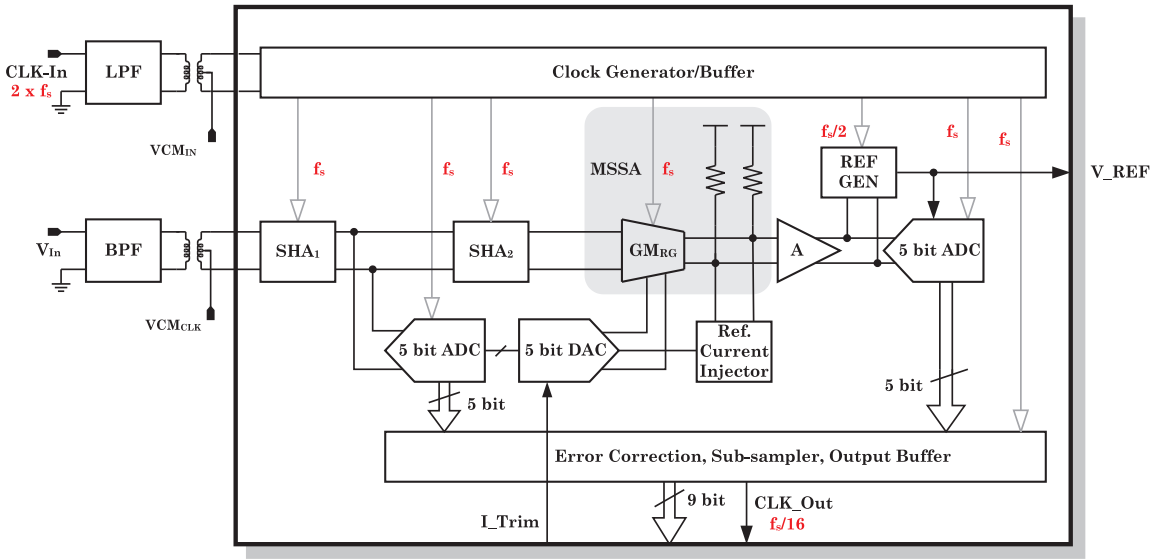


Figure 56: Block diagram of the test setup.

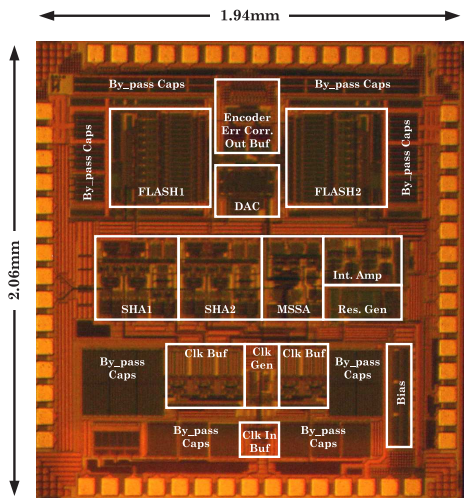


Figure 57: Photograph of the ADC chip.

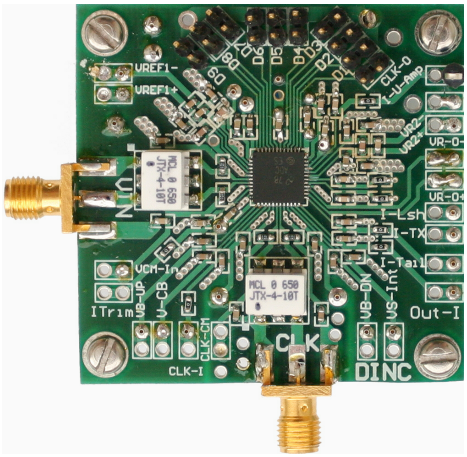


Figure 58: Photograph of the PCB used during the testing of the ADC.

The measured static metrics of the ADC is shown in Figure 60. The DNL is within ±0.8 LSB. The INL, on the other hand, stays within ±1.65 LSBs. The spectrum of the ADC output is given in Figure 61. The harmonics of the input are below -60 dBc level. However, the images of the input are visible in the spectrum. This indicates a coupling between the sampling clock of the reference-generator circuit and the input. Note that, the reference-generator circuit runs at 1/3 of the sampling frequency of the ADC and the output of the ADC is decimated by 16. Because of this coupling, the performance of the ADC and the functionality of the calibration scheme could not be

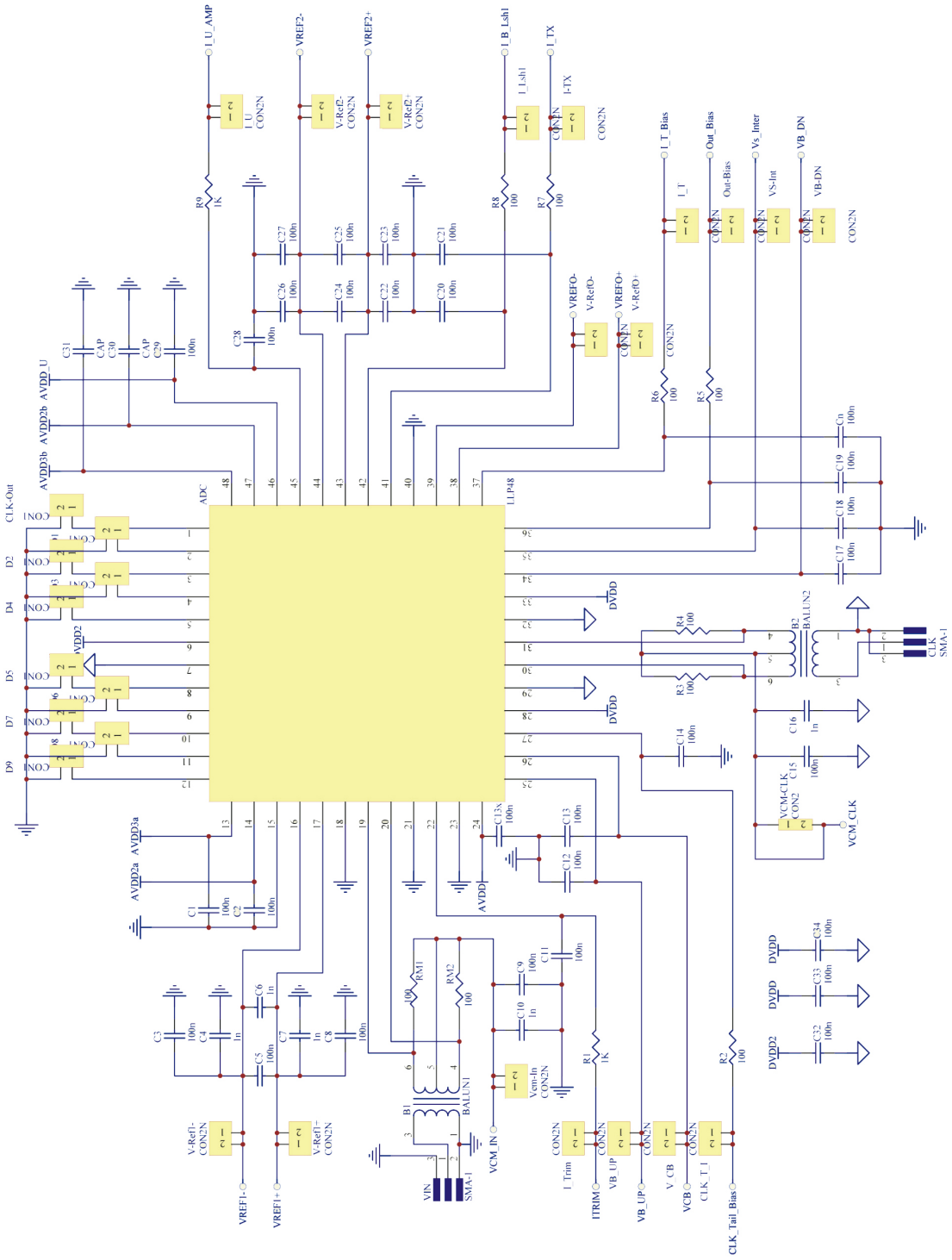
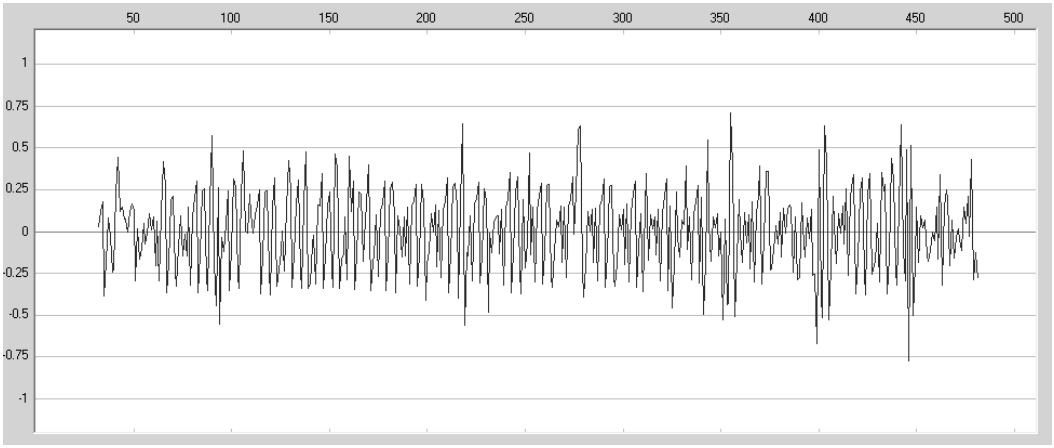
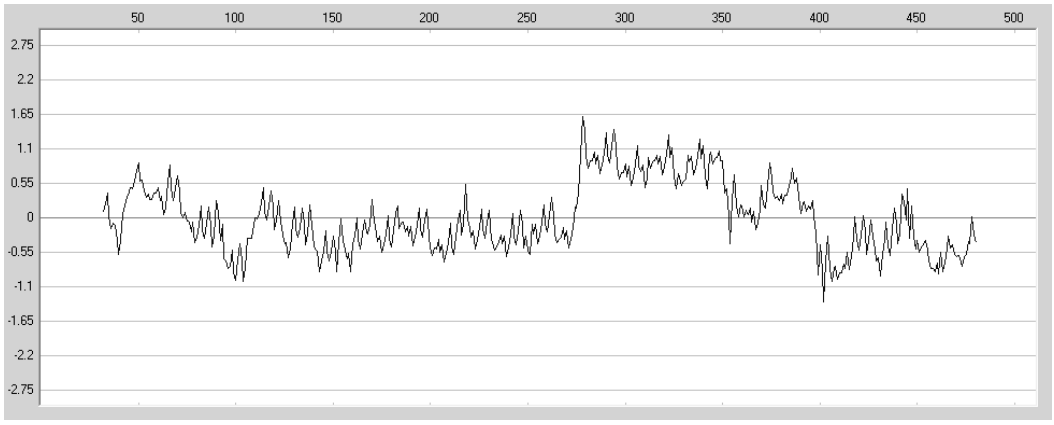


Figure 59: Schematic of the PCB used during the testing of the ADC.

fully evaluated. Therefore, the simulation results are provided as an indication of the ADC's performance without the coupling problem. Several solutions to this coupling problem are provided later. The powers of the harmonics of the ADC output are tabulated in Table 9



(a)



(b)

Figure 60: Measured static metrics of the ADC. (a) DNL. (b) INL.

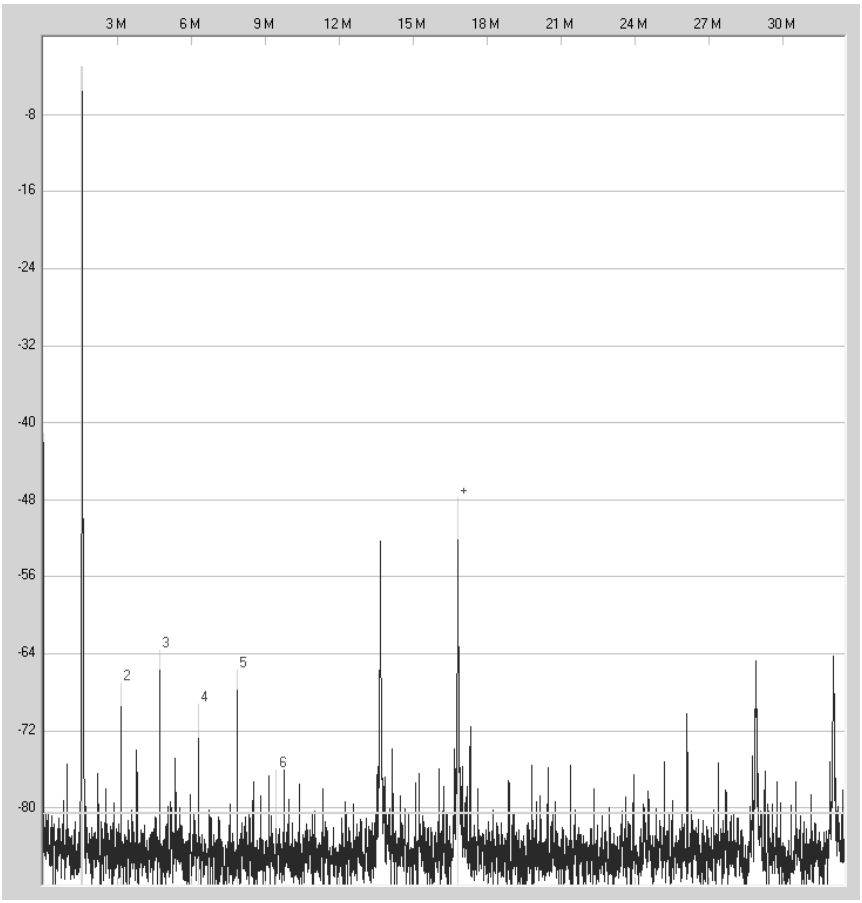


Figure 61: Measured spectrum of the ADC. The images of the input are visible in the spectrum which indicates a coupling between the analog signal and the clock of the reference generator circuit. The clock of the reference generator clock runs at 1/3 of the ADC clock.

Table 9: Levels of the Harmonics Seen in Figure 61

Harmonic	**Power (dBc)**
HD2	-65.6
HD3	-61.3
HD4	-69.5
HD5	-63.8
HD6	-79.2
Worst Other	-47.8

The performance summary of the ADC is provided in Table 10. 11.

Table 10: Performance Summary of the ADC Chip

Specification	**Comment**	**Value**
Process	CMOS	0.18 μm
Supply Voltage	Digital	1.8 V
	Analog	3.3, 1.8 V
Analog Input	–	400 mV_{pp}
Max. Clock Freq.	–	750 MHz
$HD_{2,3,4,5}$	-3 dB_{FS} Input	$>$ 60 dB
SFDR*	-3 dB_{FS} Input	$<$ 47 dB
Resolution	-	9 Bits
DNL	-	$\pm$0.8 LSB
INL	-	$\pm$1.7 LSB
Power Dissipation	Single SHA	183 mW
	Single Flash	126 mW
	DAC	8 mW
	MSSA	112 mW
	Int. Amp.	116 mW
	Ref. Gen	17 mW
	Clk. Buf.	160 mW
	Total	1.031 W

* SFDR is dominated by the coupling from the reference-generator block.

5.6 Comparison of the Designed ADC with Other Work

Although today's fine-line technologies provided more efficient designs than this work, the presented design is comparable to other designs in similar processes. Since, only NMOS transistors and telescopic-cascode structures are used to maximize speed, the power consumption was sacrificed. If low V_T devices and folded structures are used, the analog supply voltage can be reduced. Consequently, the power dissipation can be reduced. Further, some blocks, such as SHAs can run at twice the speed of this ADC. Nonetheless, their speed was not scaled down when they were copied from the SHA chips.

The main significance of this ADC is the demonstration of a pipelined ADC with an open-loop residue amplifier. This design is compared with other ADCs in similar processes in Table 11.

Table 11: Comparison of the Designed ADC with Other Work

Res.	**F_S (MHz)**	**V_{FS} (V)**	**V_{Sup} (V)**	**P (mW)**	**Process**	**FOM2 (pJ/Conv**	**Ref.**)
9	750	0.4	3.3, 1.8	1031	0.18 μm CMOS	2.7	This Work
10	500*	0.41	1.8	600	0.18 μm CMOS	1.2	[67]
8	800*	0.4	1.8	774	0.18 μm CMOS	3.8	[13]
8	1000	1	5	2500	0.5 μm Bipolar	9.8	[68]
8	600	2	3.3, 1.8	200	0.18 μm CMOS	1.3	[23]
8	2000	0.4	3.3	3500	SiGe	6.8	[69]
6	600	0.4	1.8	105	0.18 μm CMOS	2.7	[70]

* These designs are interleaved. The speed reported in this table is the speed of a single ADC

5.7 Issues and Possible Solutions

The images of the input in the measured spectrum in Figure 61 suggests that there is a coupling related to the slow clock used in the reference generator block, see Figure 56. It is observed that, the images were not present when the input signal was within a sub-range of Stage1. This coupling can be due to:

1. Layout introduced parasitic coupling
2. Timing skew on the clock signals
3. Supply glitches
4. Substrate coupling

The coupling prevented a full evaluation of the ADC's performance by degrading SFDR and the noise floor. However, the reference voltage generated by the reference generator block matched the simulations relatively well.

5.7.1 Layout Introduced Parasitic Coupling

Even though individual blocks and certain signal paths were simulated with layout parasitics, the ADC chip as a whole could not be simulated with layout parasitics due to the excessive simulation times (simulation result given in Figure 51 took a week to finish without layout parasitics on a Sun Ultra 30 computer.) The coupling due to layout introduced parasitics can be avoided with running post-layout simulations on faster computers.

5.7.2 Timing Skew on the Slow Clock Signals

Timing skew may cause overlapping condition between the slow clock used in the reference-generator block and the clock that switches the MSSA from common mode to differential mode, see Figure 46. This condition may glitch the output of the interstage amplifier (input of Stage2) at a bad instant of the amplify phase. For example, the switching glitch introduced by the reference generator block should die out before Stage2 makes a conversion, otherwise the conversion of Stage2 will be distorted by this glitch every 3rd conversion. Note that, the slow clock used in the residue generator block runs at $f_s/3$ while the ADC is clocked at f_s.

The clock skew problem could be solved by trimming the delay on the slow clock used in the reference generator block. In industry, extreme care is taken for such clocks and many bits of trim are dedicated to align critical clocks. The simulations without parasitics show a 250 ps timing difference between the edges of the clock used in the MSSA and the slow clock used in the reference generator block. Simulations with layout parasitics could have highlighted the sensitivity of clock lines to parasitic loading.

5.7.3 Supply Glitches

There are several different supply domains on the ADC chip, and these supply lines have finite impedances associated with them. Therefore, any glitch introduced to the supply lines can appear at the output of a circuit if its power supply rejection ratio (PSRR) is not high. Since many of the blocks used in this design rely on resistive loads to achieve gain, the output common-mode values track the variations on the positive

supplies. The supply glitches can cause problems by 2 different mechanisms. 1) If there is a mismatch between the load resistors, the common-mode disturbance caused by supply glitch can be converted to differential disturbance. This problem, is less of a concern because of the relatively large resistor sizes and the common-centroid layout techniques used. 2) The common-mode variation induced to the output of one block by the supply glitches can be converted to differential disturbance by the following block. This is because, CMRRs of many blocks in this design are not high enough, especially, at high frequencies due to the limited output impedances of their tail currents. Also, common-mode to differential-mode conversion is aggravated because the signal swing experienced by the input differential pairs of many blocks are relatively large.

The resistances of the supply lines were estimated by hand calculations, and they were designed to be low enough. However, supply-line and bond-wire inductances were not taken into account. The supply-line and the bond-wire inductances can cause significant supply bounce. The ADC chip was not simulated in the presence of supply impedances. More by-pass capacitors and down bonds should have been used to alleviate this problem.

5.7.4 Substrate Coupling

Substrate coupling from the reference-generator block to the main ADC blocks can cause the images in Figure 61. The proximity of the reference-generator block to the interstage amplifier, Figure 57, might be causing coupling through the substrate. This problem could be addressed by increasing the spacing between the residue-generator

block and the main ADC blocks.

5.7.5 Improving the Robustness of the Calibration

Some sort of randomization can be used to break the periodicity of the coupling from or to the calibration blocks. The randomization process can be applied at two places. 1) The sampling of the injected calibration signal. 2) The value of the injected calibration signal. The simplest way of randomizing the injected calibration signal is to randomly change its sign while keeping its amplitude same. This operation is similar to chopping in low-noise amplifier designs. However, the chopping operation is controlled with a random number generator. The following briefly describes these methods.

5.7.5.1 Randomization of the Calibration Signal Sampling

The coupling problems mentioned above can be alleviated if the period of the slow clock used in the reference-generator block is randomized, see Figure 62. With randomized sampling, the distortion caused by the coupling is randomized. Therefore, the spurs caused by the coupling are smeared into the noise floor.

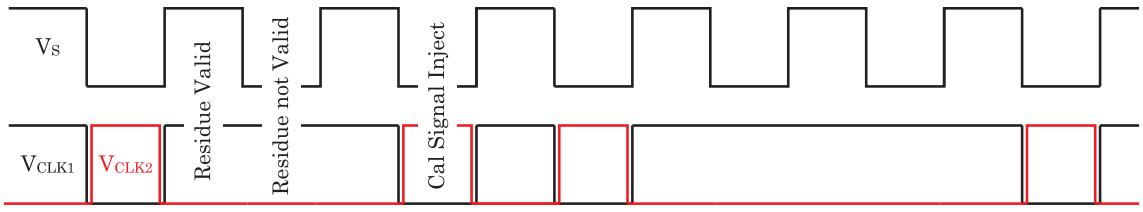


Figure 62: Demonstration of the randomized clocking in the calibration scheme.

Note that, even though randomizing the period of the slow clock used in the reference generator improves SFDR, it degrades the noise floor because the power of the spurs are distributed to the Nyquist bandwidth. Therefore, any coupling

mechanism must be carefully identified, and coupling from different sources must be minimized to limit the SNR degradation.

5.7.5.2 Randomization of the Injected Calibration Signal

Randomization of the calibration signal improves the accuracy of the calibration by improving the immunity of the injected signal to coupling. A simple example of a randomized calibration signal injection is shown in Figure 63. In this example, the sign of the injected calibration signal is randomly changed by a pseudo-random number generator. The sign of the sampled calibration signal is multiplied by the same pseudo-random number sequence to restore the correct sign of the sampled signal. Note that, while the sign of the sampled calibration signal is restored, any coupling on the the injected calibration signal is randomized. Therefore, filtering removes the distortion caused by coupling, and the calibration becomes more robust to coupling. The implementation shown in 63 is similar to the correlation technique used in [27, 40, 42]. However, in this discussion, the correlation is done in an analog fashion.

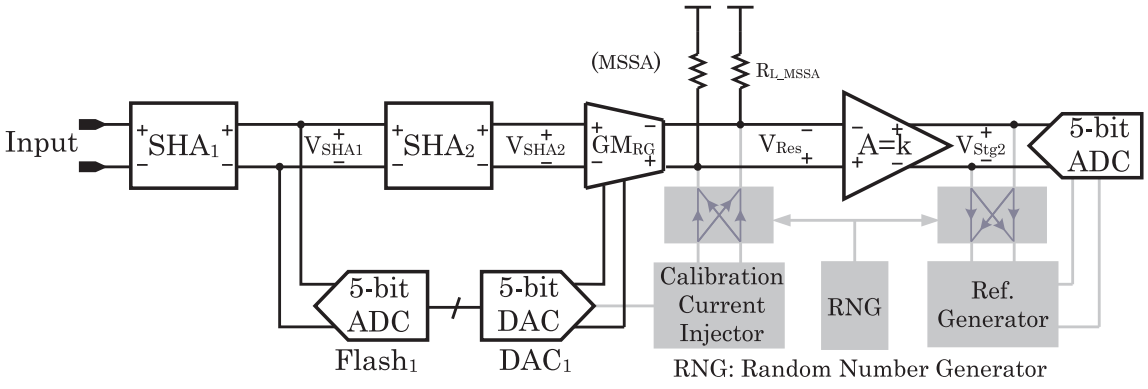


Figure 63: Demonstration of the random calibration signal injection and sampling.

5.8 Significance of This Work in Terms of Speed and Power Consumption

As explained in Section 2.4, a pipelined ADC is a cascade of low-resolution ADCs. The residue amplifier cascading the first stage, see Figure 64, must satisfy the most stringent accuracy, linearity, and speed requirements after the front-end SHA, input buffer, etc. Therefore, it may limit the speed and resolution of the overall ADC, [1, 2, 54].

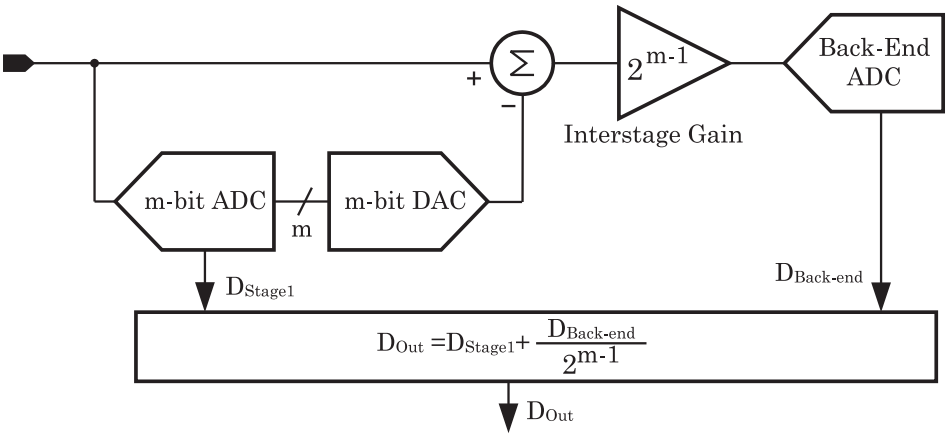


Figure 64: A simple block diagram of a pipelined ADC.

The interstage amplifier is classically designed with a high-gain amplifier operated under negative feedback. Thereby, the gain is determined by the passive feedback network, and highly-linear and low-drift gain can be guaranteed. However, high loop gain is necessary to achieve high closed-loop-gain accuracy. To obtain high open-loop gain, cascode topologies and low current densities must be used. On the other hand, high-speed operation requires high current densities and simple amplifier topologies, [56, 57, 71]. As a result, achieving high gain (high accuracy) compromises speed and vice versa.

The calibration method proposed in this research and calibration methods proposed by [27, 33, 39, 40, 66] attempt to alleviate the gain-accuracy (and linearity) requirements in the interstage amplifier. Thereby, the gain-accuracy and speed requirements in an interstage amplifier can be decoupled. This decoupling can allow the usage of open-loop interstage amplifiers if the linearity requirements are satisfied, see Figure 65.

In a high-resolution pipelined ADC, the linearity requirements of the first few interstage amplifiers may not be satisfied by an open-loop amplifier. In that case, the interstage amplifier can be a closed-loop topology with sufficient loop gain to guarantee the desired linearity. However, the deficiency of gain accuracy can be corrected by calibration. Even in this case, the amplifier's topology can be significantly simplified compared to an amplifier which must satisfy the gain accuracy requirements. The simplification in the amplifier's topology may improve speed and save power. Since a simpler amplifier has fewer roots in its transfer function, it is easier to satisfy a certain phase margin at a given GBW product. For example, with relaxed open-loop gain requirements, a simple 2-stage amplifier may be enough to get the necessary linearity as opposed to a 2-stage amplifier with a cascode, or regulated cascode first stage, see Figure 65.

Further, the transfer function of the interstage amplifier can be corrected in a nonlinear fashion as discussed in Section 5.2.6.1, and [33, 39]. In that case, not only the gain accuracy but also the linearity requirements of the interstage amplifier can be relaxed. Calibration for nonlinearity compensation may further result in simplification in the amplifier's topology, and using a simple differential pair with resistive

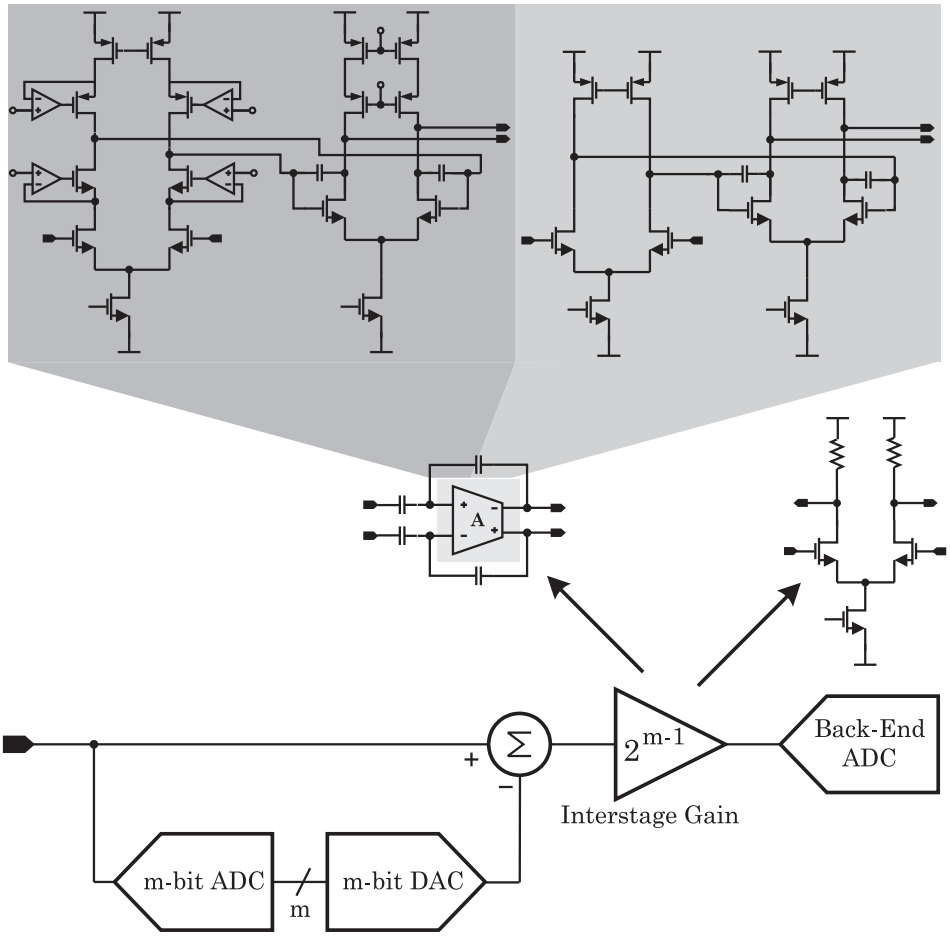


Figure 65: Possible amplifier topologies that can be used in the interstage amplifier.

loads may suffice for medium resolutions as explained in this work and [72].

5.8.1 Comparison of 2-Stage Amplifier and Resistively-Loaded Differential Pair

The 2-stage Miller amplifier has been a popular amplifier architecture for its simplicity, and ability to provide high dynamic range, open-loop gain and speed. In this section, a 2-stage Miller amplifier is quantitatively compared to a resistively-loaded differential pair. This comparison is done to highlight the benefits of using an open-loop amplifier and correcting its disadvantages with calibration instead of using a closed-loop amplifier with very-high loop gain. Since, the calibration method

described in [33, 72] corrects the shortcomings of an open-loop interstage amplifier, similar comparisons are done in [72]. The simplified schematics of the 2-stage amplifier and the resistively-loaded differential pair compared in this section, are given in Figure 66.

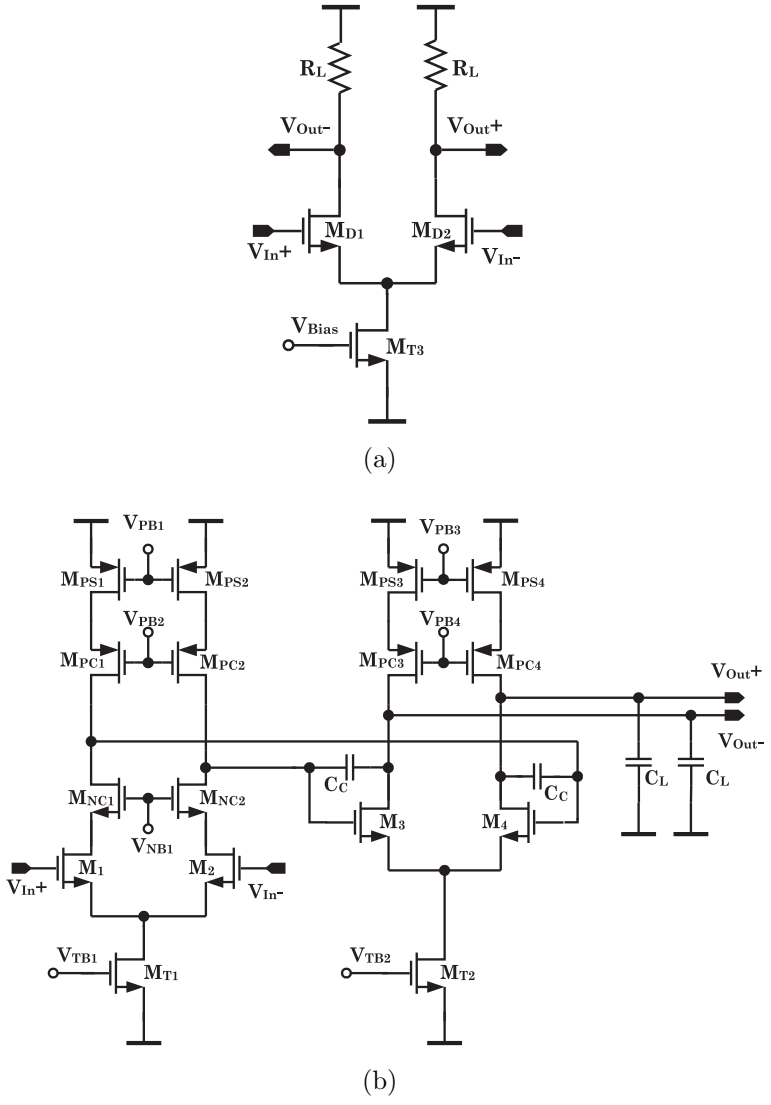


Figure 66: Schematics (a) Resistively-loaded differential amplifier. (b) 2-stage amplifier.

The GBW product of a Miller amplifier is given by:

$$\mathrm{GBW_{Miller}} = \frac{\mathrm{gm_1}}{\mathrm{C_C}}, \tag{41}$$

where $\mathrm{gm_1}$ is the transconductance of transistor $\mathrm{M_1}$ and $\mathrm{C_C}$ is the compensation capacitor. As a rule of thumb, an amplifier has to have better than 45° phase margin to guarantee stability under closed-loop operation. Needless to say, in reality, the phase margin should be much better than 45° to provide minimum settling time with a given GBW. For the sake of simplicity, the second pole (output pole) is assumed to be at 3×GBW, and all other roots are ignored in this comparison. This condition results in 75° phase margin. With this assumption, the second pole, $\mathrm{P_2}$, is given by:

$$\mathrm{P_2} = \frac{\mathrm{gm_3}}{\mathrm{C_L}} = 3 \times \mathrm{GBW_{Miller}}, \tag{42}$$

where $\mathrm{gm_3}$ is the transconductance of transistor $\mathrm{M_3}$ and $\mathrm{C_L}$ is the load capacitor.

On the other hand, the gain ($\mathrm{A_{Dif}}$), BW, and GBW of the resistively-loaded differential pair are:

$$\mathrm{A_{Dif}} = \mathrm{gm_{D1}} \times \mathrm{R_L}, \tag{43}$$

$$\mathrm{BW_{Dif}} = \frac{1}{\mathrm{R_L} \times \mathrm{C_L}}, \tag{44}$$

and

$$\mathrm{GBW_{Dif}} = \frac{\mathrm{gm_{D1}}}{\mathrm{C_L}}, \tag{45}$$

where gm_{D1} is the transconductance of transistor M_{D1} and R_L is the load resistor.

Note that, the output pole and many other roots in its transfer function limit the phase margin of a 2-stage amplifier. This is especially true if multiple cascode topologies and gain-boosting techniques are used to achieve high open-loop gain. Therefore, the GBW product has to be limited to achieve the desired phase margin and settling behavior.

As a conclusion, the maximum achievable speed in a closed-loop system is limited by its stability requirements. The speed of an open-loop system, on the other hand, is not limited by stability requirements. Therefore, an open-loop system can provide a higher GBW product with the same load, see Equations 41 and 45.

Several parameters of the 2-stage amplifier and the resistively-loaded differential pair shown in Figure 66 are compared in the following. Same GBW is assumed for both circuits.

5.8.1.1 Power Comparison

The 2-stage amplifier discussed above has a power consumption of:

$$P_{2Stage} = 2\left(I_{M1} + I_{M3}\right) V_{DD} = 2V_{DD}\frac{V_{od}}{2}\left(C_C + 3C_L\right) GBW. \tag{46}$$

where I_{M1} and I_{M2} are the currents running through M_1 and M_3 respectively, and V_{od} is their overdrive voltage. For the sake of simplicity, V_{od} is assumed to be same for M_1 and M_3.

On the other hand, the power consumption of the resistively-loaded differential pair with the same GBW is given by:

$$P_{Dif} = 2I_{D1}V_{DD} = 2V_{DD}\frac{V_{od}}{2}C_L GBW. \tag{47}$$

where I_{D1} is the currents running through M_{D1}. Again, for the sake of simplicity, V_{od} of M_{D1} is assumed to be same as V_{od} of M_1 and M_3.

5.8.1.2 Noise Comparison

The 2-stage amplifier utilizes more transistors than a resistively-loaded differential pair to achieve high open-loop gain. Therefore, it is expected to be noisier. The noise of the 2-stage amplifier is given by, [55–57]:

$$V^2_{N-2Stage} = 2\left[\alpha\frac{4kT}{gm_1} + \alpha\frac{4kT}{gm_{PS1}}\left(\frac{gm_{PS1}}{gm_1}\right)^2\right] + V^2_{N-Stg2} \approx 2\alpha\frac{4kT}{gm_1}\left(1 + \frac{gm_{PS1}}{gm_1}\right). \tag{48}$$

where gm_{PS1} is the transconductance of transistor M_{PS1}, k is the Boltzmann's constant, T is the absolute temperature, and α is a scaling factor. Note that, the second-stage noise, V^2_{N-Stg2}, can be ignored, since it is attenuated by the gain of the first stage. Also, the PMOS current source, M_{PS1}, can be a significant source of noise if its V_{od} is designed relatively low for headroom reasons. Note that, low V_{od} results in larger gm with a given drain current.

The noise of the resistively-loaded differential pair is:

$$V^2_{N-Dif} = 2\left[\alpha\frac{4kT}{gm_{D1}} + \frac{4kT}{R_L}\frac{1}{gm^2_{D1}}\right] = 2\alpha\frac{4kT}{gm_{D1}}\left(1 + \frac{1}{\alpha A_{dif}}\right). \tag{49}$$

It can be seen from Equation 49 that for a sufficiently large A_{dif}, the input-referred noise of the resistively-loaded differential pair is dominated by the input devices.

Finally, several parameters calculated for the 2-stage amplifier and the resistively-loaded differential pair are summarized in Table 12.

Table 12: Comparison of 2-Stage Amplifier and Resistively-Loaded Differential Pair

Parameter	**2-Stage Amplifier**	**Differential Pair**
GBW*	$\frac{gm_1}{C_C}$	$\frac{gm_{D1}}{C_L}$
Power	$V_{DD}V_{od}\left(C_C + 3C_L\right)GBW$	$V_{DD}V_{od} \times C_L \times GBW$
Noise	$2\alpha\frac{4kT}{gm_1}\left(1+\frac{gm_{PS1}}{gm_1}\right)$	$2\alpha\frac{4kT}{gm_{D1}}\left(1+\frac{1}{\alpha A_{dif}}\right)$

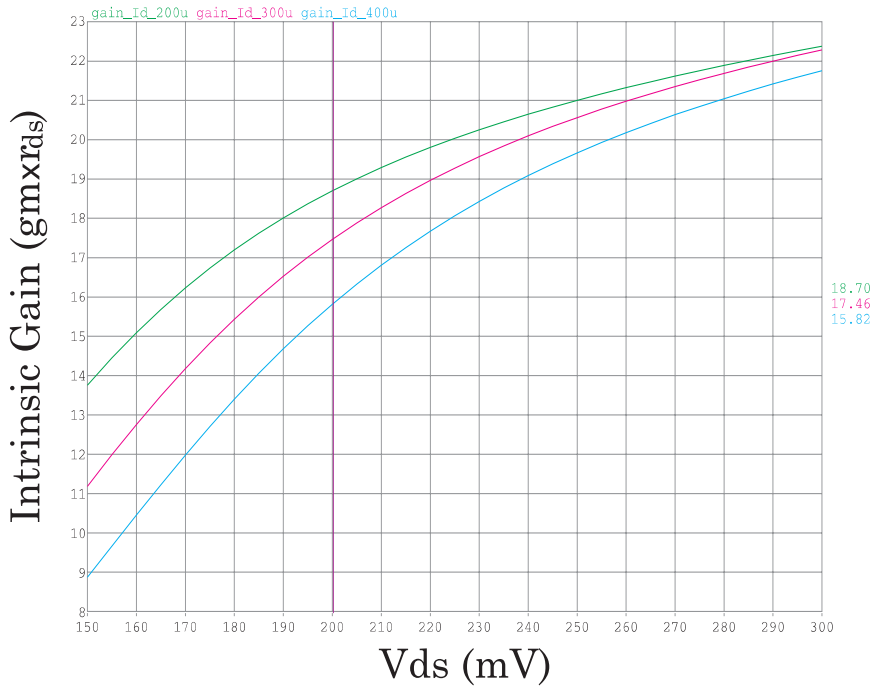
* The GBW product of the 2-stage amplifier is limited by stability requirements. However, there is no such restriction for the resistively-loaded differential pair.

It is clear from Table 12 that resistively-loaded differential pair out performs the 2-stage amplifier in every parameter. However, a heavy toll is paid in terms of accuracy and linearity. None the less, the proposed calibration method and other calibration techniques introduced by [27, 33, 39, 40, 42, 66, 72] alleviate the accuracy and linearity problems.

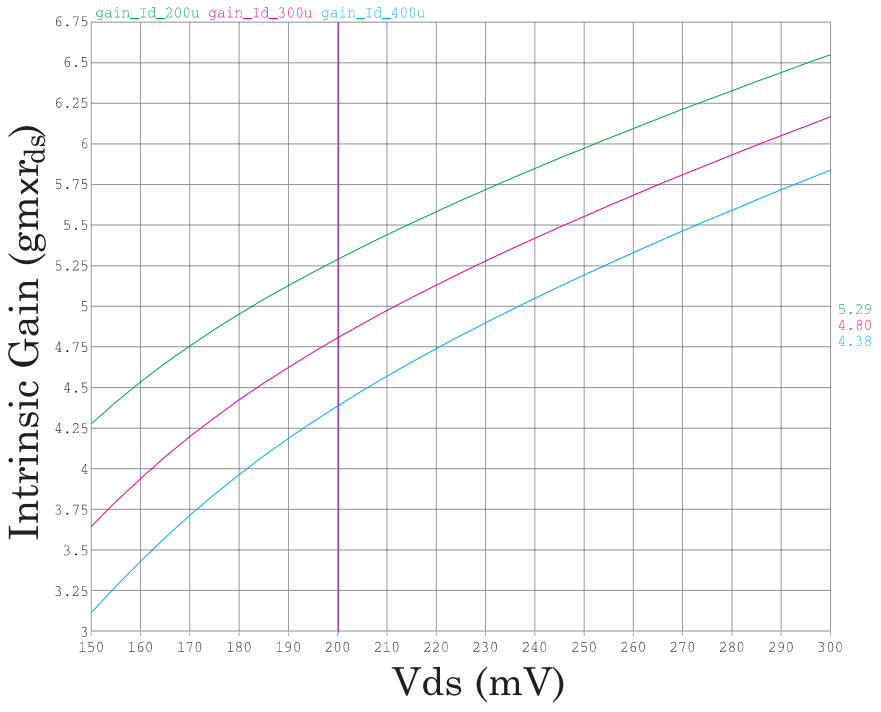
5.9 Significance of This Work for Fine-Line CMOS Technologies

The intrinsic gain ($gm \times r_{ds}$) of MOS transistors reduces as the gate lengths shrink with the introduction of each new process node. The reduction in intrinsic gain is mainly caused by increased channel length modulation and drain induced barrier lowering. Figure 67 plots the intrinsic gain of NMOS transistors versus drain-to-source voltage in a 0.18 μm and 65nm CMOS processes. The transistor aspect ratios are selected to keep the current densities same.

If we examine the region where the drain-to-source voltage is between 150-250



(a)



(b)

Figure 67: Intrinsic gain (gm × r_{ds}) of NMOS. (a) In a 0.18 μm process. (b) In a 65 nm process.

mV, it can be seen from Figure 67 that the intrinsic gain of the NMOS in the 65 nm process is about 1/3 of the one in the 0.18 μm process. With this information in hand, it is worthwhile to calculate the gain that can be achieved by a 2-stage amplifier with a cascoded first stage.

In the 0.18 μm process, the gain of a 2-stage amplifier with a cascoded first stage is:

$$A_{0.18\mu m} \approx (gm \times r_{ds})^3 = 18^3 = 5800 = 75dB. \tag{50}$$

The same amplifier topology in the 65 nm process can provide the following gain:

$$A_{65nm} \approx (gm \times r_{ds})^3 = 5^3 = 125 = 42dB. \tag{51}$$

A typical closed-loop switched-capacitor interstage amplifier is shown in Figure 68. It is useful to calculate the accuracy limit of the back-end stage, if these amplifiers are used to implement the interstage amplifier.

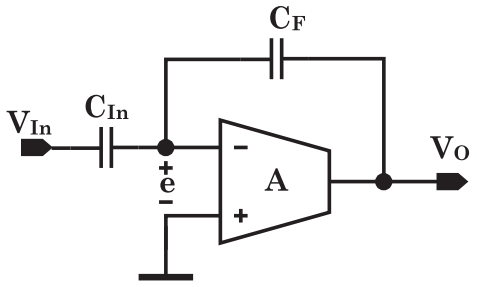


Figure 68: A simplified schematic of a closed-loop interstage amplifier.

First, we need a relation that expresses the closed-loop gain in terms of the open-loop gain and closed-loop gain (or feedback factor). The output voltage, V_O is given by:

$$V_O = -V_{In}\frac{C_{In}}{C_F + \frac{C_{In}+C_F}{A}} = -V_{In}\frac{a_{CL}}{1+\frac{1+a_{CL}}{A}} \tag{52}$$

where A is the open-loop gain of the amplifier shown in Figure 68 and a_{CL} is the closed-loop gain with infinite open-loop gain (i.e. the ideal gain of the interstage amplifier.) Using Equation 52, we can derive that for an N-bit back-end resolution, the open-loop gain of an amplifier used in the interstage amplifier must satisfy the condition given by Equation 53 to guarantee less than 1/2 LSB gain error.

$$A \geq (a_{CL}+1)\left(2^{N-1}-1\right). \tag{53}$$

Plugging the open-loop gain values obtained for the amplifier in the 0.18 μm and 65nm processes into Equation 53, we can calculate the achievable back-end resolutions in each process: The back-end resolution in the 0.18 μm process can be 7 bits for an interstage gain of 16, i.e. a 5-bit first stage. However, the same amplifier topology with the same interstage gain allows a 2-bit back-end stage in the 65 nm process. It is obvious that in the 65 nm process, the gain of the amplifier must be improved by multiple cascode topologies or gain boosting techniques, which limit speed. The other alternative is to rely on calibration and relax the gain accuracy requirements.

As a conclusion, calibration can improve speed in older process technologies by allowing the usage of simple amplifier topologies. On the other hand, calibration has to be used in fine-line processes not only for its benefits for speed but also to satisfy gain-accuracy requirements, which are adversely affected because of the low intrinsic device gain.

5.9.1 Performance Projections of the Designed ADC in Faster CMOS Processes

5.9.1.1 Bandwidth Scaling

Most of the blocks in this design rely on resistive loading to achieve gain. The bandwidths of these resistively-loaded stages are determined by their load resistors and input capacitance of the following stages.

$$\mathrm{BW} = \frac{1}{\mathrm{R_L C_L}} = \frac{1}{\mathrm{R_L C_{Gate-Next}}}, \tag{54}$$

The input capacitance of the stages can be estimated using the definition of transit frequency, $\mathrm{f_T}$, [56, 57]:

$$\mathrm{f_T} = \frac{\mathrm{gm}}{2\pi \mathrm{C_{Gate}}}, \longrightarrow \mathrm{C_{Gate}} = \frac{\mathrm{gm}}{2\pi \mathrm{f_T}} \tag{55}$$

where gm is the transconductance of the device and $\mathrm{C_{Gate}}$ is the total capacitance seen from the gate. Equation 55 suggest that the value of the load capacitance decreases as $\mathrm{f_T}$ increases. Therefore, assuming the load resistors are kept constant, BW of the circuits used in this design scale with $\mathrm{f_T}$ as shown in Equation 56.

$$\mathrm{BW} = \frac{1}{\mathrm{R_L} \times \mathrm{C_{In-Next}}} \propto \frac{\mathrm{f_T}}{\mathrm{R_L}}. \tag{56}$$

Consequently, assuming the load resistors are kept constant, technology scaling directly translates into speed improvement.

5.9.1.2 Power Scaling

For speed comparison, we assumed that the load resistors are kept constant across processes; therefore, the transconductances of the devices must be kept constant to keep the voltage gains constant. Assuming that the transistors obey the square-law model, keeping the transconductances same suggests using lower bias currents in finer process. However, in reality short channel effects and increased doping densities in finer processes reduce mobility, and the transconductance efficiency, gm/I_D, reduces [73,74]. None the less, loss in transconductance efficiency can be recovered by slightly increasing the transistor aspect ratios. Consequently, bias current can be assumed to stay constant, if the design is migrated to a finer process.

More over, in fine-line CMOS processes there are many flavors of transistors with different V_T levels. This aspect of the finer technologies may allow a better optimization of headroom, and consequently supply voltage and power consumption.

5.9.1.3 Summary of the Performance Projection of the ADC in a 65 nm Process

In this section, the power consumption and speed of this design will be projected in a 65nm process. As discussed in section 5.9.1.1, speed of this design directly scales with the f_T of the process. The f_T versus V_{od} of an NMOS transistor in the 0.18 μm and 65 nm processes are shown in Figure 69. The aspect ratio of the transistor is kept constant. It can be seen that the f_T of the 65 nm process is roughly 3.5 times the f_T of the 0.18 μm process within the region where V_{od} is between 150 - 250 mV. Therefore, the same ADC designed in this 65 nm should be able to run at 2.6 GSample/s.

On the other hand, as discussed in section 5.9.1.2, it is safe to assume that a block

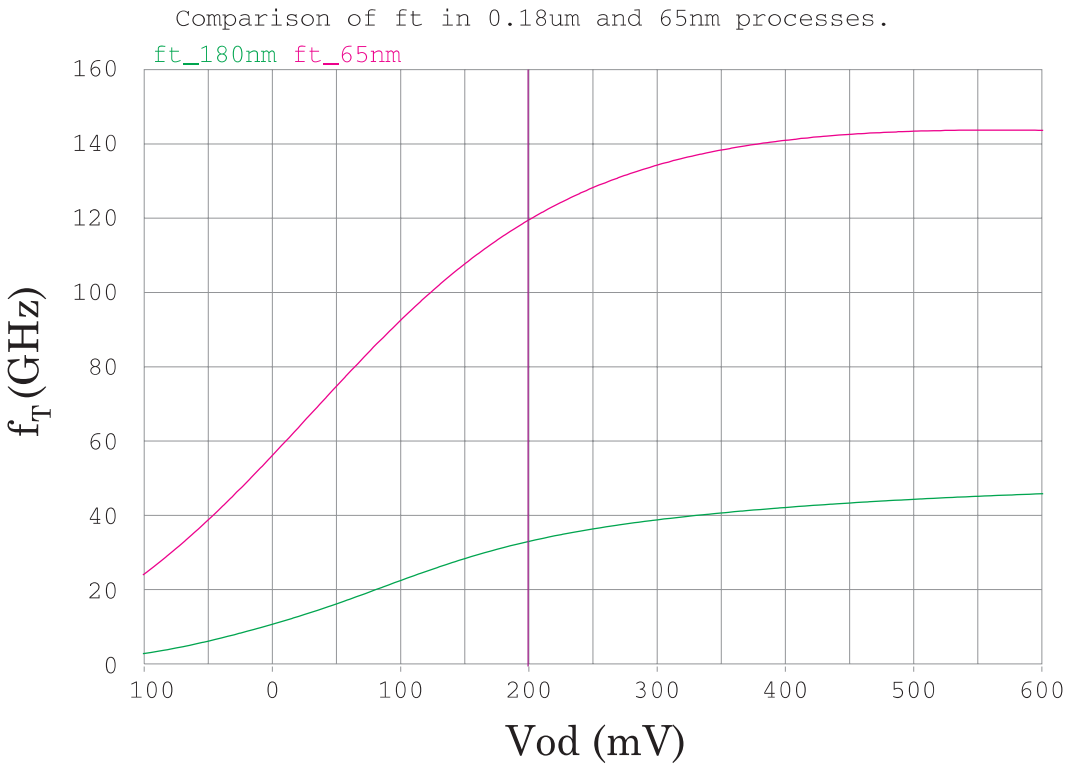


Figure 69: Comparison of f_T in 0.18 μm and 65 nm proceses.

biased from a 3.3 V (1.8 V) supply in the 0.18μm can be biased from a 2.5 V (1.2 V) supply in the 65 nm process. Estimation of power dissipation of various blocks used in this ADC are compared for the 0.18 μm and 65 nm processes in Figure 70. Figure 71 is the Walden chart including this ADC's performance in two processes.

As a conclusion, if this ADC is designed in a 65 nm process, the bias currents can be kept same and the design can fully benefit from the speed improvement provided by the process. The power, on the other hand, will have a less aggressive scaling, and it will scale with the scaling of the nominal supply voltages specific to the used process. In this discussion, the objective was to maximize conversion speed; however, the other extreme case can be to minimize power while keeping the conversion speed same.

Table 13: Comparison of ADC's Performance in a 0.18 μm and 65 nm Process

Process	Conversion Speed	Power
0.18 μm	750 MSample/s	1.03 W
65 nm	2.6 GSample/s	758 mW

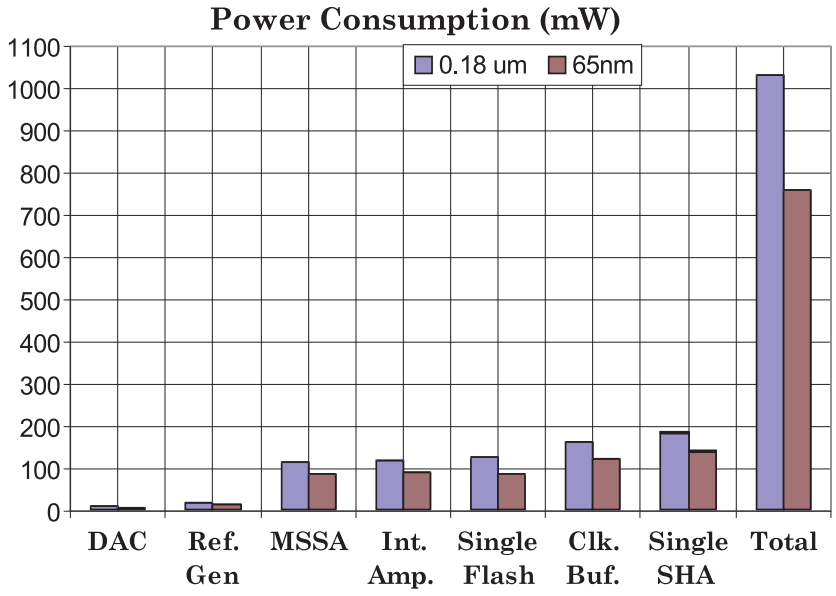


Figure 70: Comparison of power consumption in 0.18μm and 65 nm proceses.

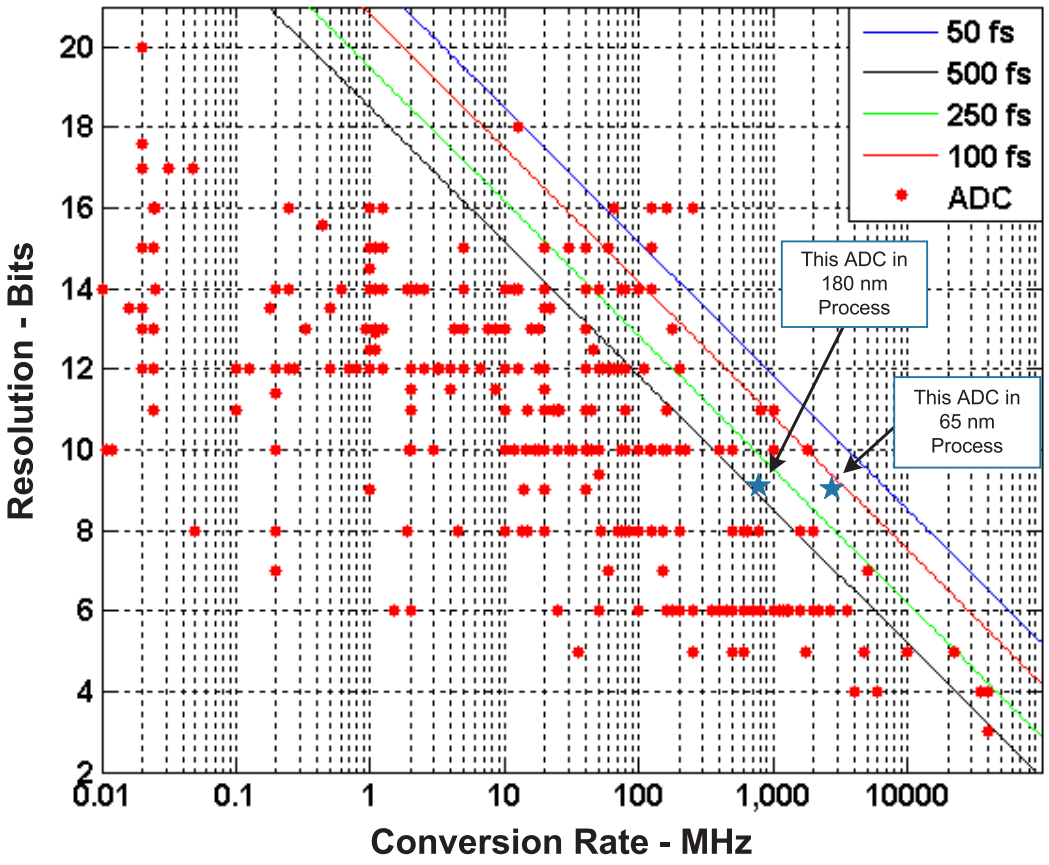


Figure 71: Comparison of this ADC with other ADCs on the Walden chart.

5.10 Summary

The main design considerations of the proposed two-step ADC are provided with the schematics, and relevant simulation and experimental results. Extensive simulations have shown that the performance of the building blocks are sufficient for the intended 9-bit accuracy up to 750 MHz conversion rate. The high-frequency operation is made possible by local-feedback circuits, current-mode operation, and the open-loop residue amplifier. Further, the design utilizes a front-end SHA to alleviate timing requirements between Flash1 and SHA_2 at the expense of power consumption, signal-to-noise ratio and die area.

A background calibration method is proposed to generate the reference for Stage2. The proposed method alleviates the performance deterioration caused by variations in the gain of the interstage amplifier. Therefore, the interstage amplifier used in this design could have an open-loop architecture. The proposed background calibration depends on scaling the reference of Stage2 by the same factor that scales the gain of the interstage amplifier. This is done by forcing the output of the residue generator to a known voltage when the residue generator and interstage amplifier are not required for residue generation and amplification respectively. During this phase, the forced voltage is amplified by the interstage amplifier. The output of the residue amplifier is sampled, filtered, and amplified by a predetermined gain to generate the reference of Stage2. The reference-generator circuit samples, filters, and amplifies the output of the interstage amplifier when the output of the residue generator is forced to a known voltage.

The reference-generator circuit is clocked at a different frequency than the main clock frequency to save power. Measurements have shown that, this clock mixes with the analog signal and generates images. This can be avoided by randomizing the period of the clock used in the reference generator, which can smear the image tones into the noise floor.

The proposed calibration method is realized purely in the analog domain, which made the implementation more cumbersome and susceptible to device parameters, coupling, etc. More sophisticated, however similar, methods can be implemented in the digital domain with better accuracy, and immunity to noise and coupling. Finally, the calibration method proposed can be improved to correct for the nonlinearities of the interstage amplifier.

CHAPTER VI

A RAIL-TO-RAIL SLEW-RATE-BOOSTED PRE-CHARGE BUFFER

6.1 Introduction

Delta-sigma (Δ-Σ) and successive approximation (SAR) ADCs can achieve high accuracies at low sample rates with relatively low power consumption. These attributes make them natural choices for sensor interface applications. The input sampling networks of the SAR, Δ-Σ, and pipelined ADCs are typically switched-capacitor circuits. The switching nature of these input sampling networks can introduce memory and cause distortion if the source driving the ADC has a large source impedance. The distortion caused by input sampling networks gets worse as the sampling rates increase and/or as the value of sampling capacitor increases.

A viable approach to alleviate the distortion caused by the input-sampling network is to buffer the input with a highly linear buffer, [66]. However, it is extremely difficult for a buffer to have a better linearity than high-resolution Δ-Σ converters with acceptable power consumption. Instead, a pre-charge buffer can be used to charge the input capacitor of a switched-capacitor circuit close to the input voltage in a small fraction of the sampling (acquisition) phase [75, 76]. After the pre-charging period, the input can be directly connected to the sampling capacitor and fine settling can be achieved over a switch. The pre-charging action significantly reduces the current

supplied by the source. Therefore, the effective input impedance of the switched-capacitor circuit increases. In the following section, the design considerations of a pre-charge buffer are discussed.

6.2 Overview

The sampling nature of the switched-capacitor technique demands large transient currents from the source to charge and discharge the input sampling capacitor. A simple way to alleviate this problem is to buffer the input. However, a highly linear input buffer is difficult to design, and may result in excessive power and area consumption. An alternative to a linear input buffer is a pre-charge buffer. A pre-charge buffer, whose function is to charge the input sampling capacitor in a small fraction of the sampling phase is a coarse buffer with a high slew-rate. After the coarse pre-charging phase, accurate settling is achieved over a MOS switch in the remainder of the sampling phase, see Figure 72.

6.3 Circuit Design

In this design, the pre-charge buffer is realized with a linear amplifier, which operates under unity-gain negative feedback. Since the input range is rail-to-rail, the input and output of the amplifier must be able to handle rail-to-rail signals. This requirement, on the other hand, has its own well known problems such as varying transconductance over the input range, distortion caused by cross over, etc. The pre-charge buffer was optimized for maximum 1 MHz clock frequency. The pre-charge phase was designed to be about 1/8 of the total sampling phase. Therefore, the amplifier must be fast enough to settle within a reasonable accuracy in about 60 ns.

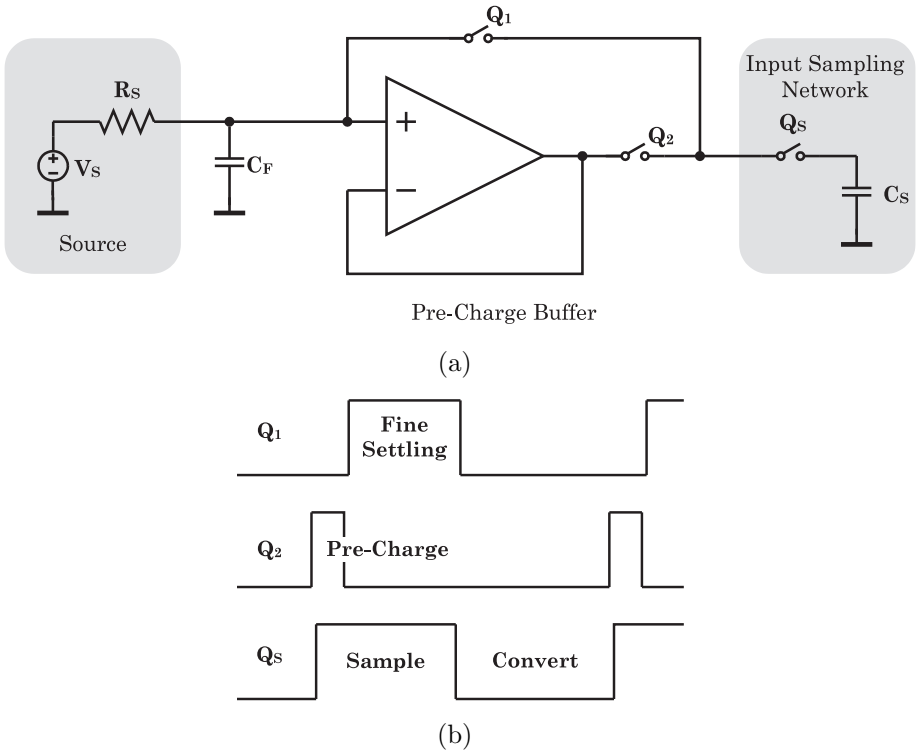


Figure 72: The concept of pre-charging to alleviate kick-back from the sampling capacitor. (a) Block diagram. (b) Clocking scheme.

6.3.1 Architecture

The current mirror OTA [55–57] was adapted as the linear amplifier. A complementary NMOS-PMOS input stage was utilized to extend the input common-mode range. A simplified schematic of the pre-charge buffer is shown in Figure 73. The main parameters that determine the settling behavior of an OTA are gain-bandwidth product (GBW) and slew-rate (SR). The GBW and SR of this OTA are given by

$$\mathrm{GBW} = \mathrm{n}\frac{\mathrm{GM_N} + \mathrm{GM_P}}{\mathrm{C_L}} \tag{57}$$

and

$$SR = \frac{2I_T}{C_L} \tag{58}$$

respectively, where **n** is the mirroring ratio between the input transconductance and the output branch, GM_N and GM_P are the transconductances of NMOS and PMOS differential pairs, C_L is the load capacitance, and I_T is the tail current. The tail currents of the NMOS and PMOS input pairs are designed to be the same.

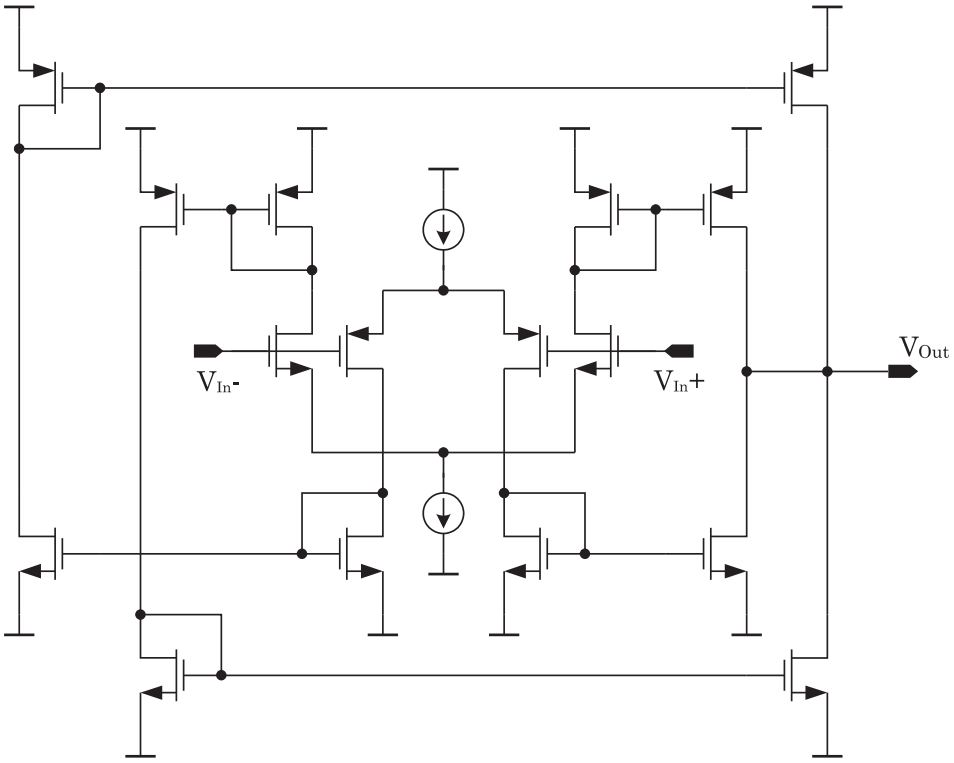


Figure 73: Simplified schematic of current mirror OTA with complementary inputs.

The OTA shown in Figure 73 has a fixed slew-rate, whose value is determined by the tail-current sources and the mirroring ratio. Therefore, a slew-boosting mechanism is required to enhance the settling performance without dissipating excessive power. The slew-rate can be enhanced by increasing the tail current when the circuit starts slewing. The slew-rate can be boosted significantly just by increasing the

tail current because there is no significant topological limitation to increase the tail current (for example, a folded cascode OTA has topological limitations as far as the value of tail current is concerned. The cascode device must be kept in saturation for proper operation.)

Since the input structure of the OTA is a complementary NMOS-PMOS differential pair, the amplifier can be seen as two amplifiers with NMOS and PMOS input stages operating in parallel as shown in Figure 74. As a result, one amplifier can be optimized towards one rail, and the other for the other rail. For instance, the positive slew-rate of the amplifier can be optimized by optimizing the slew-rate of the amplifier with the NMOS input stage. The negative slew-rate, on the other hand, can be optimized by optimizing the slew-rate of the amplifier with the PMOS input stage. Furthermore, slewing can be detected by comparing the currents at the branches of the input differential pair. This detection can be realized easily, which will be explained in the following.

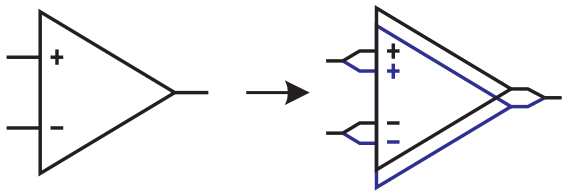


Figure 74: The amplifier can be seen as two amplifiers operating in parallel.

6.3.2 The Slew-Rate Boosting Mechanism

For the sake of simplicity, the amplifier with the NMOS input stage is discussed in this section. The same comments apply to the amplifier with the PMOS input stage with dual transistors and quantities. The schematic of the amplifier with the NMOS

input stage is given in Figure 75. The transistors M_1-M_8 comprise the current-mirror OTA, the remaining transistors function within the slew-rate boosting mechanism. The circuit utilizes two different positive feedback loops to boost the slew-rate in either direction. The transistors M_{13}- M_{15}, and M_{BU} boost the positive slew-rate. On the other hand, transistors M_9-M_{12} and M_{BD} boost the negative slew-rate. The slew-rate is determined by the negative slew-rate of the amplifier with NMOS input stage if the input is close to the positive rail. Note that, when the input is close to the positive rail, the amplifier with the PMOS input stage is not functional. Therefore, the amplifier with the NMOS input stage requires negative slew boosting when the input is close to the positive rail. This operating region covers an input range about 1 V from the positive rail.

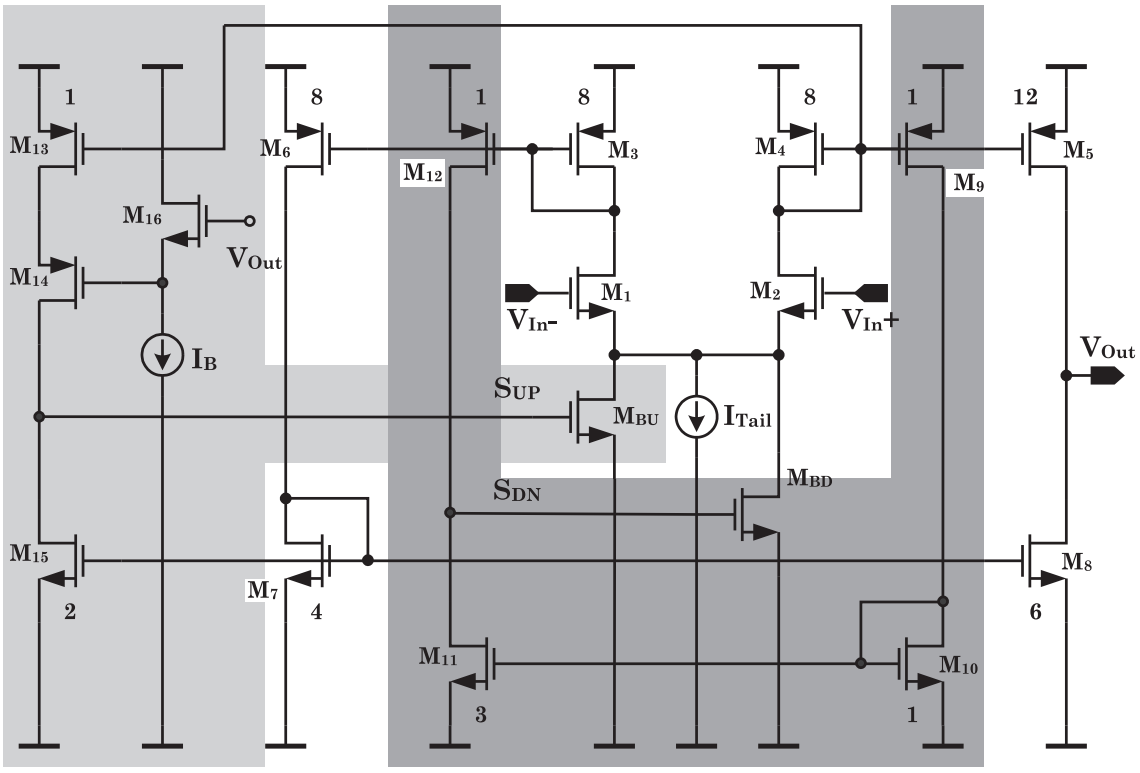


Figure 75: Schematic of the OTA with NMOS input stage.

The negative slew-boosting loop is naturally shut down by the NMOS input pair. However, the loop boosting the positive slew-rate is deactivated by M_{16} to avoid any unpredictable operation incase input exceeds the positive rail. The positive slewing condition is determined by comparing 1/8 of the current through M_2 with 1/2 of the current through M_1. This comparison is achieved with the mirrored currents through M_{13} and M_{15}. The difference in the comparison quantities ensure that the slew-boosting loop is deactivated under linear operation conditions. When the input is close to the output, the gate of M_U is low because the current through M_{15} is four times the current through M_{13}. Consequently, M_{15} operates in linear region. As the input voltage increases rapidly, the output cannot track the input. Therefore, current through M_1 increases, whereas the current through M_2 decreases. The pull-down power of M_{15} weakens while the pull-up power of M_{13} gets stronger. After a critical value, M_{BU} turns on, and starts contributing to the tail current thereby increasing the slew-rate. Since the loop uses positive feedback, the output voltage increases until M_{15} forces M_{BU} to cut off. If the input step is sufficiently large, the gate of M_U hits the positive rail and boosts the tail current tremendously. This condition necessitates a mirroring device (M4) with a large aspect ratio (M_3 for the negative slew boost) otherwise M_2 enters the linear region, pulls down the source of M_1 and increases its current, which pulls the SUP node to the negative rail. Consequently, the circuit exits the slew-boosting condition prematurely.

The amplifier with NMOS input stage does not need to be functional for the input values close to the negative rail. Therefore, NMOS mirrors M_{8-7-15} and M_{10-11} are small devices. The slew-boosting loops enhance the drive capability of the circuit

significantly. However, the circuit slews for sometime with the inherent slew-rate before the slew-boosting loops are activated. The inherent slew-rate is set by the tail current. Therefore, inherent slewing time can be reduced if the quiescent tail current is increased. Moreover, the transistor sizes (parasitic capacitors) should be reduced to increase the inherent slew-rate and speed up the slew-boosting mechanism.

Phase margin and output-signal handling capability are some other design criteria to consider. With fixed tail current, the bandwidth reduces by half when the input is close to either rail because one of the amplifiers is disabled. To alleviate this problem, the tail current of one of the amplifiers is doubled as the other amplifier shuts down. Doubling the tail current significantly improves the settling time of the functioning OTA even though the GBW is reduced compared to the condition in which the two OTAs operate in parallel. This is a result of the improvement of the inherent slew-rate of the active OTA due to the increase in its tail current.

The schematic of the bias circuit realizing tail-current doubling is given in Figure 76. The operation of the circuit can be explained as follows: The current through M_{B8} consists of two components, which are the currents through M_7 and M_4. When the input common mode is not close to the positive rail, the current through M_4 is half of the current through M_7. As the input common mode approaches to the positive rail, the transistors M_{B1} and M_{B1} force M_{B6} into linear region. Consequently, the current through M_{B4} reduces to zero. As a result, the current through M_{B8} doubles. A dual replica of this circuit biases the amplifier with PMOS input stage.

When the pre-charge buffer is not used, the tail currents of the amplifiers are reduced to 1/10 of their quiescent value to save power. This reduction is performed

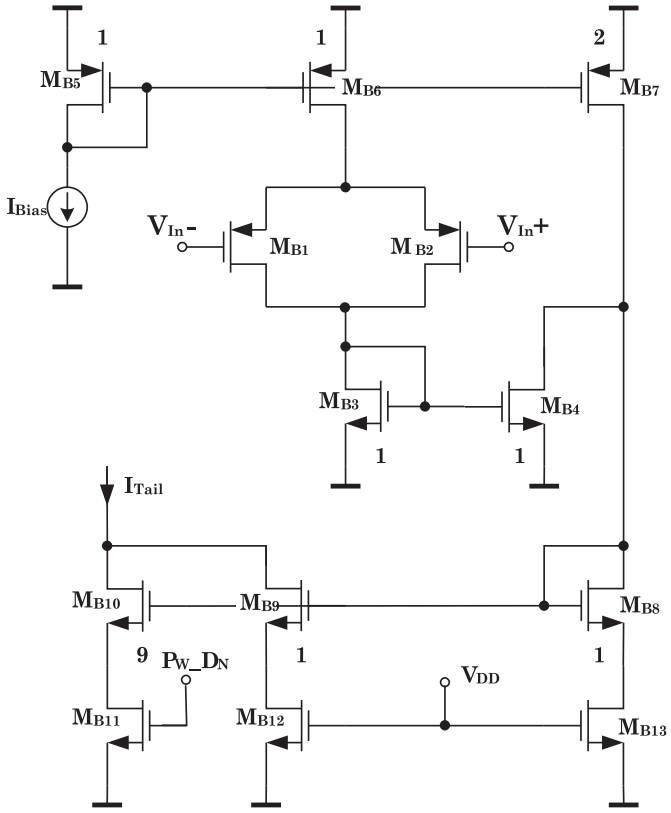


Figure 76: Tail current doubler. The transistors M_1 and M_2 are scaled versions of input differential pair.

by transistors M_{9-12}. A small amount of current is left to bias the OTA in power-down mode to speed up the power-up. There are no stability problems under power-down-mode operation as the current mirror OTA is a self compensated one. Further, the slew-boosting mechanism is disabled under power-down condition.

6.3.3 Simulation Results

Various simulation results are provided in this section. Figure 77 shows the frequency response of the OTA with different process corners at different temperatures. The large signal (rail-to-rail) settling of the OTA is provided in Figure 80 with different process corners at different temperatures. The settling behavior with smaller steps at different input common-mode voltages is also provided in Figure 79.

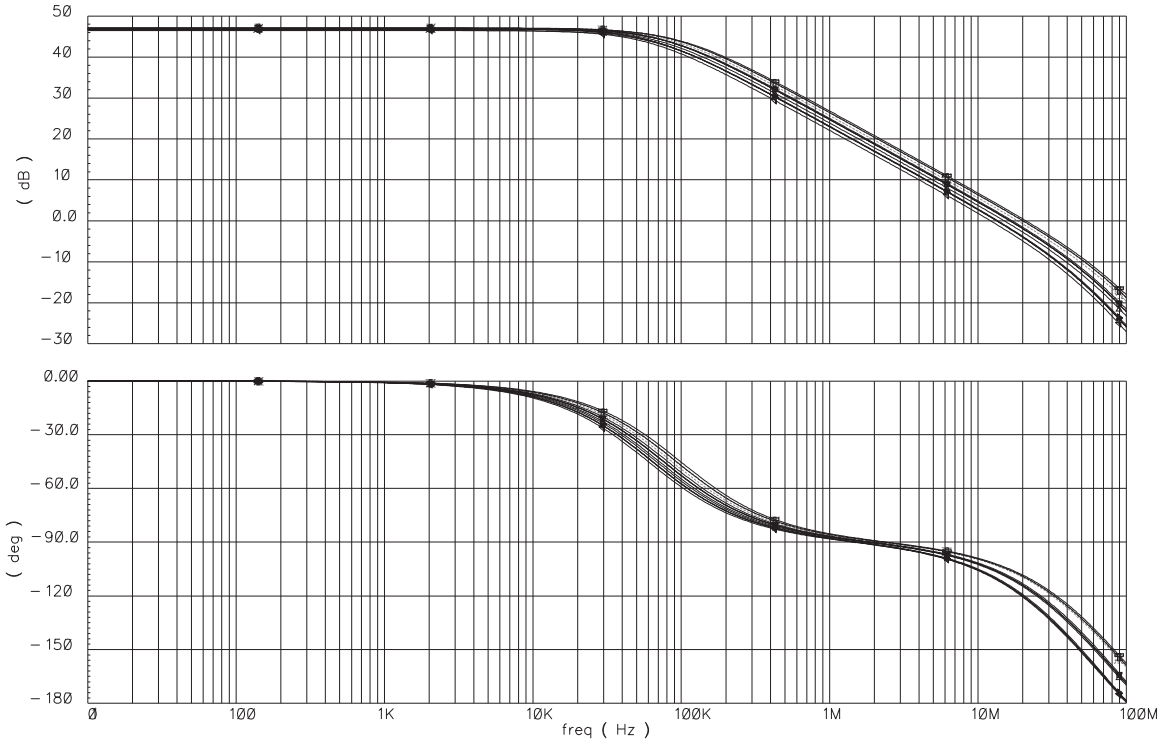


Figure 77: Frequency response with different process corners at different temperatures.

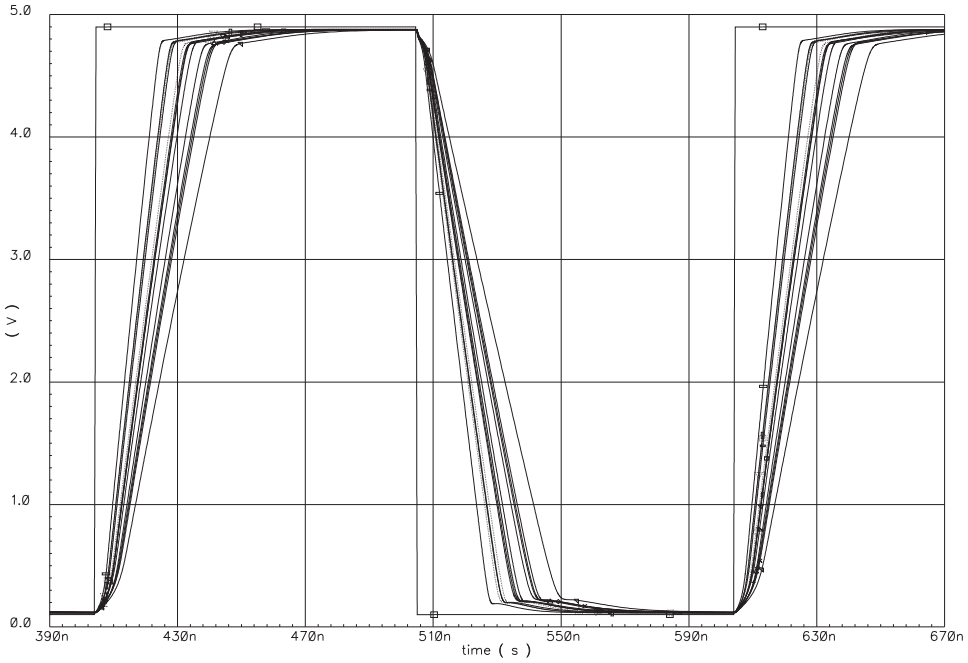


Figure 78: Large signal (rail-to-rail) settling behavior with different models at different temperatures.

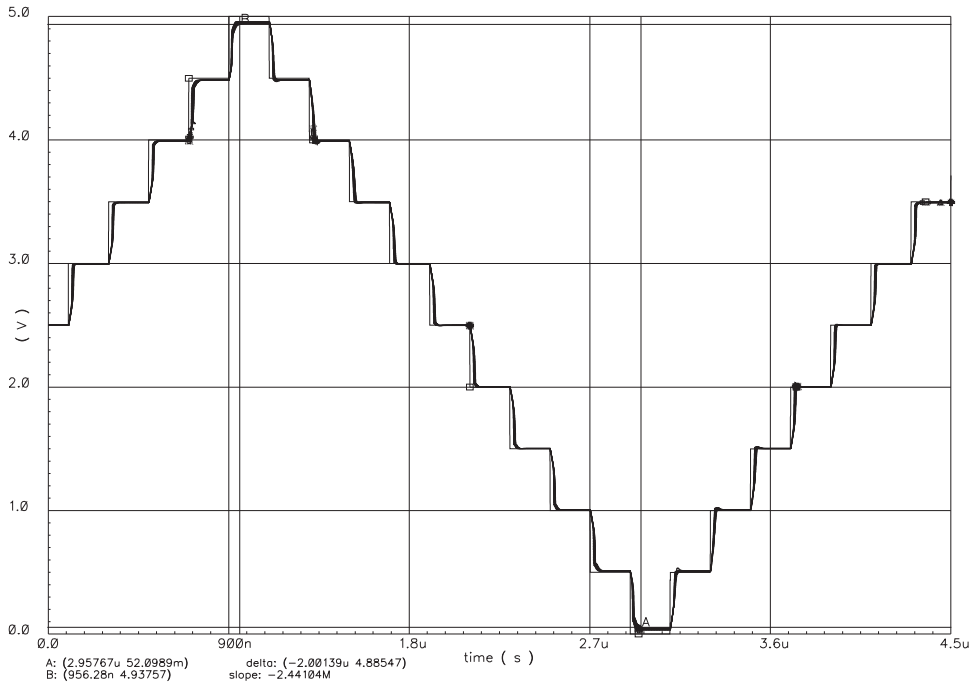


Figure 79: Large signal settling behavior at different common mode voltages with different models at different temperatures.

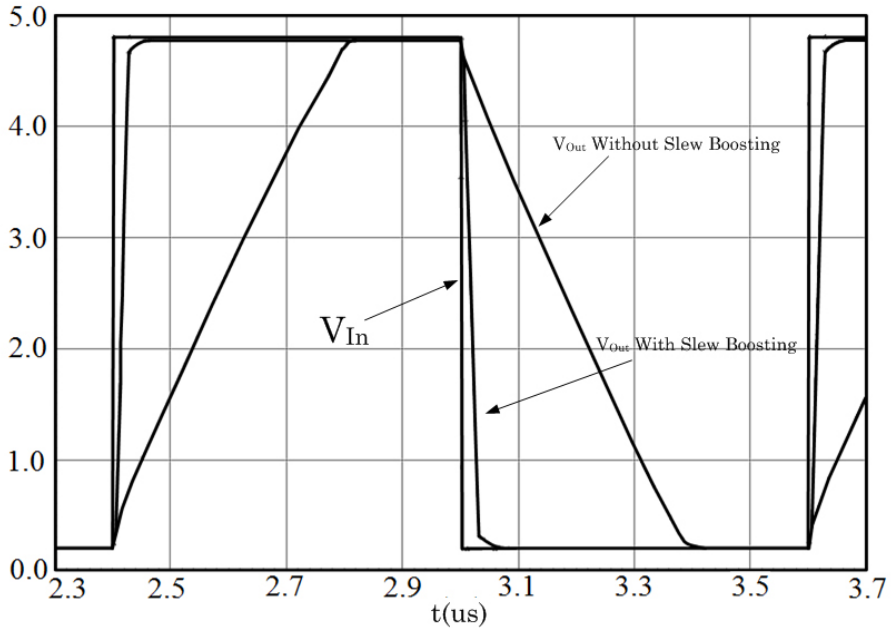


Figure 80: Large signal settling with and without slew boosting.

The effect of the slew-rate-boosting mechanism on the settling time is shown in Figure 80. Finally, Table 14 provides a summary of the important parameters of the pre-charge buffer.

Table 14: Performance Summary of the Pre-Charge Buffer

Quantity	**Condition**	**Value**
GBW	Typical model, room temperature	13 MHz
Bias Current	Nominal operation	265 μA
	Power down mode	79 μA
Slew-Rate	Slew boost on, $C_L = 8$ pF	156 V/μs
	Slew boost off, $C_L = 8$ pF	10.5 V/μs
Settling time	$< 2\%$ accuracy	< 60 ns
Input CMR		Rail to rail
Output Swing	With capacitive load	Rail-to-rail

6.4 Summary

A pre-charge buffer was designed and simulated in a 0.5 μm CMOS process. The buffer achieves better than 2% settling accuracy in 60 ns with 8 pF load capacitor and 265 μA quiescent current. The slew-boosting mechanism is shown to improve the large-signal settling significantly. Moreover, the circuit does not exhibit overshot due to the current-mode slew-sensing technique. The circuit successfully uses positive feedback to boost slew-rate. The positive-feedback loop is disabled by the negative-feedback loop as the output voltage converges to the input voltage, and the pre-charge buffer returns to linear operation.

CHAPTER VII

A CURRENT-FEEDBACK LOW-DISTORTION CMOS PROGRAMMABLE-GAIN AMPLIFIER

7.1 Introduction

Programmable-gain amplifiers (PGAs) are generally used when a high-dynamic-range signal has to be converted into the digital domain. This is a common scenario for wireless communication applications. The PGA amplifies the input signal to an appropriate level, which optimally loads the input of the ADC in the signal chain. The high sensitivity levels required by many wireless standards give rise to stringent requirements on the overall receiver noise figure. Therefore, the quantization noise of the ADCs in the receiver chain should be minimized by optimally loading the ADC by a PGA.

In this chapter, the design of a PGA for the IEEE 802.11a standard is discussed. The standard supports a variety of data rates requiring a bandwidth of 20 MHz for each channel, receiver sensitivity of -71 dBm at 64 QAM, and -85 dBm at QPSK constellation, with -25 dBm maximum RMS detectable power.

The proposed PGA architecture utilizes a low-noise amplifier (LNA) with 20 dB fixed gain, two stages of amplifiers, whose gain can be changed from 2 dB to 20 dB in 2 dB steps, and a unity gain buffer at the output. Such a topology provides flexibility in the optimization of linearity, power dissipation, noise, and area. A block diagram

of the designed PGA is given in Figure 81. The amplifier stages with programmable gains ($PGA_{1,2}$) will be referred to as PGA sub-stages.

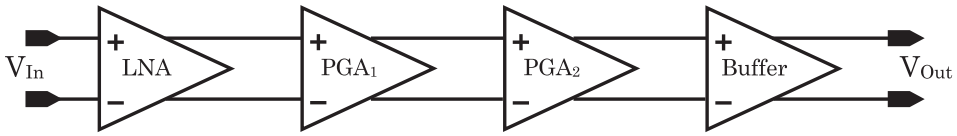


Figure 81: A simplified block diagram of the proposed PGA.

The LNA provides a better noise performance compared to the PGA sub-stages, but it has a fixed gain. On the other hand, the PGA sub-stages are noisier than the LNA. However, they are instrumental in programming the gain of the PGA. The circuit can tolerate more noise in the PGA sub-stages and the output buffer because the gain of the LNA attenuates the total noise of the PGA sub-stages and buffer referred to the input of the first PGA sub-stage, when this noise is referred to the input of the LNA.

The PGA sub-stages have to accommodate large input amplitudes when the gain of the PGA is small. Therefore the PGA sub-stages were designed to be highly linear with reasonable power consumption even when they have to handle large input amplitudes. The proposed architecture allows the optimization of the linearity of the PGA sub-stages with relatively small power and area consumption (with noisier PGA sub-stages.) However, the noise performance of the overall PGA is enhanced by utilizing a fixed-gain LNA without consuming excessive power.

The block diagram of the PGA with the necessary by-pass and signal-routing switches are provided in Figure 82. Routing the signal to different blocks can result in significant power savings and better design optimization [77, 78]. Referring to

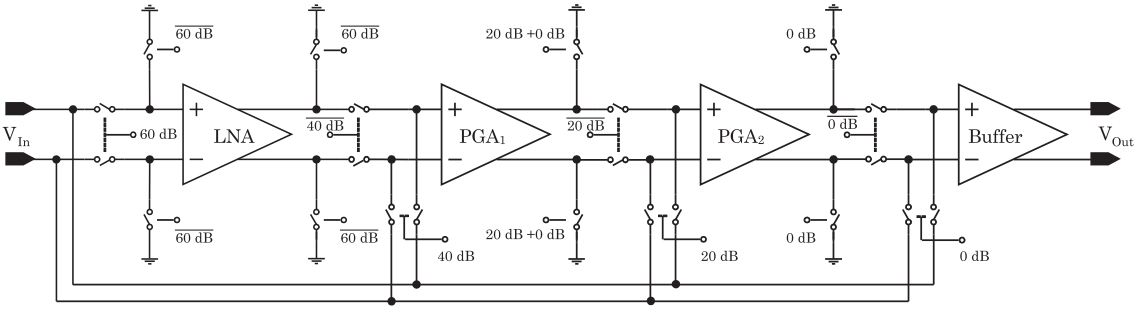


Figure 82: Block diagram of the proposed PGA with signal routing switches.

Figure 82, the operation of the PGA can be summarized in four regions as follows:

1) When the overall gain is larger than 40 dB, the LNA amplifies the input signal and feeds the amplified signal to the first PGA sub-stage. The gain programmability between 40 dB and 60 dB can be realized by changing the gain of either both or either one of the PGA sub-stages. If the switching time is critical, only one PGA sub-stage can be programmed to get the desired gain and the other PGA sub-stage can deliver a fixed 20 dB gain. In that case, either the first PGA sub-stage will have smaller gain or the second PGA sub-stage has to handle large signals. The first choice degrade noise performance. On the other hand, the second choice hurts linearity. Therefore, in this design, the gains of both PGA sub-stages are changed to keep the gain of the first PGA sub-stage and the signal level at the second PGA sub-stage at moderate levels.

2) When the overall gain is between 20 and 40 dB, the input LNA is by-passed. The inputs and outputs of the LNA are shorted to the common-mode voltage to speed up switching when the LNA has to be inserted back into the amplifier chain. The LNA could be shut down to save power. However, since the switching time was not critical, this was not attempted in this design. The gain programmability is achieved

by changing the gain of both of the PGA sub-stages. Again, to speed up switching time, the gain of only one PGA sub-stage can be programmed to get the desired gain. Further, by-passing the LNA and changing the gain of both PGA sub-stages result in better linearity while maintaining the SNR same as the first condition discussed above.

3) When the overall gain is between 2 and 20 dB, the input LNA and the first PGA sub-stage are by-passed. The inputs and outputs of the by-passed stages are shorted to the common-mode voltage. None of the stages are powered down. The gain is programmed by changing the gain of the second PGA sub-stage.

4) When no amplification is required, the input is simply routed to the output buffer by-passing all the previous gain stages. Significant amount of power can be saved if the by-passed stages are powered down or their bias currents are reduced considerably. However, these power saving methods were not implemented in this design. The following sections discuss the design of each block comprising the PGA.

7.2 Low-Noise Amplifier

The LNA consists of an NMOS differential pair with PMOS loads as shown in Figure 83. The transistors M5 and M6 provide the necessary excess current to bias the output at the desired operating point. Note that, a PMOS differential pair with PMOS loads would result in better matching (due to matching of same type of transistors) and possibly better $1/f$ noise. However, an NMOS input stage is utilized to reduce the input capacitance and improve high-frequency performance.

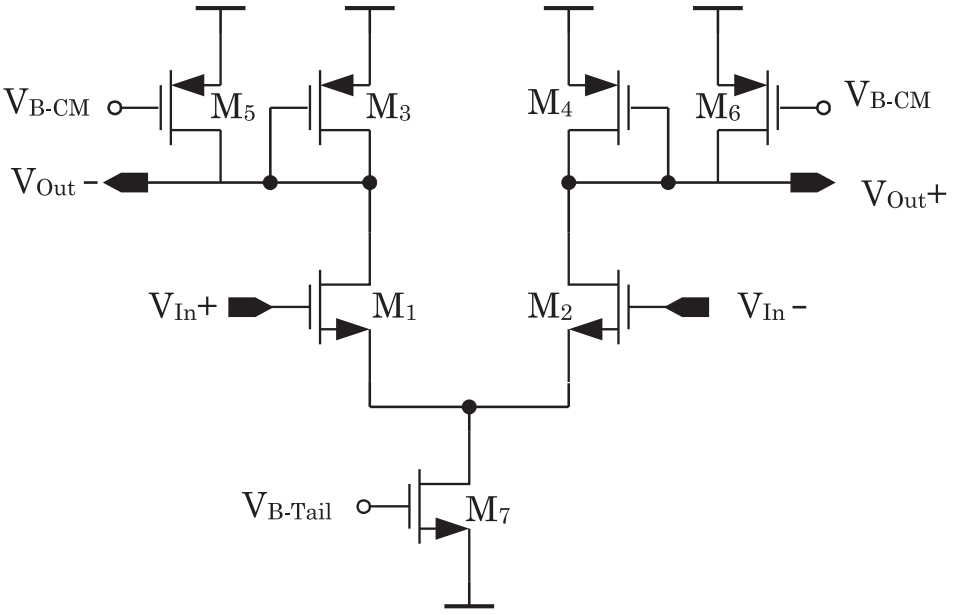


Figure 83: Schematic of the LNA.

The maximum input amplitude that has to be handled by the LNA is about 5 mV. Therefore, there are no significant constraints on the overdrives of the input transistors as far as the linearity is concerned. The overdrives of the input differential pair can be as low as 50 mV. However, to limit the area and input capacitance, the input transistors are designed to have an inversion factor of about 15, which gives a good compromise between area (input capacitance) and power consumption, [79, 80]. The sensitivity of gain in terms of device transconductances is given by

$$\frac{\sigma^2\left(\Delta \mathrm{A}\right)}{\mathrm{A}^2} = \frac{\sigma^2\left(\Delta \mathrm{gm}_1\right)}{\mathrm{gm}_1^2} + \frac{\sigma^2\left(\Delta \mathrm{gm}_3\right)}{\mathrm{gm}_3^2}, \tag{59}$$

and the noise of the LNA is given by

$$\overline{\mathrm{V}}_{\mathrm{n}} = 2\left[\overline{\mathrm{V}}_{\mathrm{n1}}^2 + \left(\frac{\mathrm{gm}_3}{\mathrm{gm}_1}\right)^2 \overline{\mathrm{V}}_{\mathrm{n3}}^2 + \left(\frac{\mathrm{gm}_5}{\mathrm{gm}_1}\right)^2 \overline{\mathrm{V}}_{\mathrm{n5}}^2\right], \tag{60}$$

where A is the gain of the LNA, $\mathrm{gm_i}$ are the transconductances of $\mathrm{M_i}$, and $\mathrm{V_{ni}}$ are

the noise voltages of M_i. In this design $gm_1/gm_3 = 10$ by design.

7.3 Current-Feedback Amplifier

The current-feedback amplifier is adapted as the PGA sub-stage because of its ease of gain programmability, high output-swing capability, and reasonable linearity. The potential of achieving high bandwidths with current feedback, [56, 81], is not emphasized in this design since the targeted -3 dB bandwidth is about 20 MHz.

The PGA sub-stage achieves 20 dB gain with about 60 dB SFDR with 1 V_{PP} differential output. The block diagram of the current-feedback amplifier is given in Figure 84. Note that, this current amplifier is a generic amplifier with conceptual differential current input and single-ended current output. The current amplifier in [81], which has a specialized input stage, should not be mistaken with this generic form.

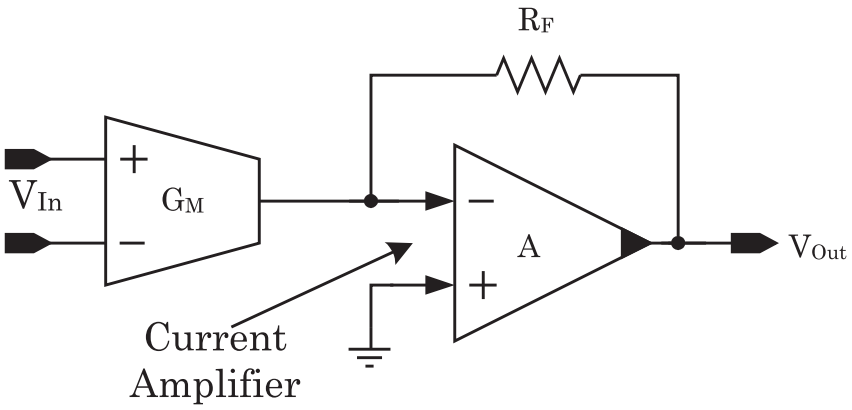


Figure 84: Block diagram of the current-feedback amplifier.

The low-frequency voltage gain of this amplifier can be expressed as

$$\frac{V_{Out}}{V_{In}} = -G_M \frac{A}{1+A} R_F, \tag{61}$$

where G_M is the transconductance of the input OTA, A is the current gain of the current amplifier, and R_F is the feedback resistor. The frequency response of the amplifier can be analyzed as follows: Assume that the current-feedback amplifier has one pole other than the output pole, and C_L is the total load and parasitic capacitance at the output as shown in Figure 85.

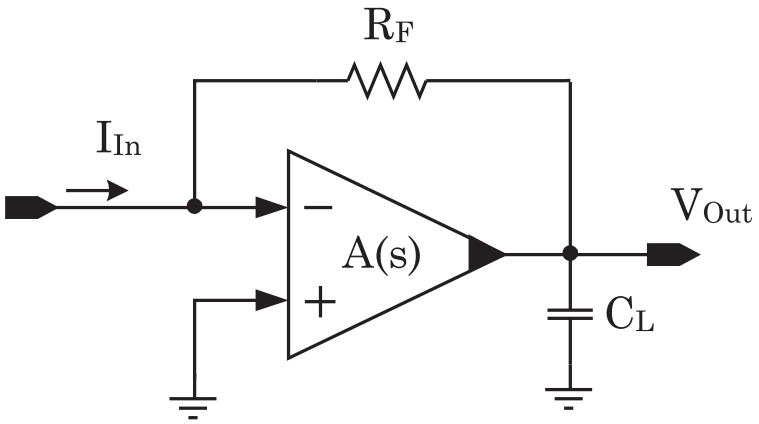


Figure 85: Block diagram of the current-feedback amplifier.

The trans-resistance gain of this amplifier can be written as

$$\frac{V_{Out}}{I_{In}} = -\frac{AR_F}{(1+A)+sC_L R_F}, \tag{62}$$

where

$$A = A(s) = \frac{A_O}{1+\frac{s}{p_A}}. \tag{63}$$

Therefore,

$$\frac{V_{Out}}{I_{In}} = -\frac{A_O p_A}{C_L} \frac{1}{s^2 + s\left(p_A + \frac{1}{R_F C_L}\right) + p_A \frac{(1+A_O)}{R_F C_L}}. \tag{64}$$

Assuming a dominant pole system, the pole locations can be calculated for the two asymptotic conditions as given in Table 15.

Table 15: Locations of the Poles of Current Amplifier for Different Approximations

Condition	$\mathbf{p_A >> p_{Out} = \frac{1}{R_F C_L}}$	$\mathbf{\frac{1}{R_F C_L} = p_{Out} >> p_A}$
Non-dominant Pole	$p_{non-d} \approx p_A$	$p_{non-d} \approx \frac{1}{R_F C_L}$
Dominant Pole	$p_d \approx \frac{1+A_O}{R_F C_L} = (1+A_O)\, p_{Out}$	$p_d \approx (1+A_O)\, p_A$
DC Gain	$\frac{A_O}{1+A_O} R_F$	$\frac{A_O}{1+A_O} R_F$
Gain Bandwidth	$A_O R_F p_{Out} = A_O R_F \frac{1}{C_L R_F}$	$A_O R_F p_A$

The real potential of the current-feedback amplifier is revealed if the amplifier is used as a voltage amplifier with a buffer at the output, i.e. when the output pole is not dominant. In this case, the GBW of the current-feedback amplifier can be increased by increasing the DC gain, which can be accomplished by increasing R_F without effecting the -3 dB frequency.

7.3.1 Gain Programmability

The gain of the PGA sub-stage is programmed in 6 dB steps by changing the G_M in 6 dB steps. Finer gain programmability is achieved by changing the gain of the PGA sub-stage in 2 dB steps by scaling R_F, see Figure 84. The complete schematic of the PGA sub-stage is provided in Figure 86. The input OTA shown in Figure 85 is realized by an NMOS differential pair with programmable transconductance as

shown in Figure 86(b). A fraction of the current generated by the input differential pair is switched to the input of the current amplifier or dumped to ground to change the gain in 6 dB steps. This results in excellent gain matching due to the large input transistors (better matching) and insensitivity to switch resistance. Also, with such a switching scheme, the intrinsic linearity capability of the current to voltage conversion at the input is not changed over the entire programmability range unlike the source degeneration scaling in [77]. Further, this topology keeps the current modulation at the current amplifier reasonably low under the entire gain levels. The current amplifier shown in Figure 85 is realized by a PMOS current mirror as shown in Figure 86(a). Using R_F to change the gain in 2 dB steps changes the bandwidth. Therefore, the value R_F must be designed for the lowest BW condition, which is the highest gain setting. In this design the BW of the PGA has to be only 20 MHz. Therefore, the PGA sub-stages are not buffered to save power. Consequently, the pole associated with the output of the PGA sub-stage is the dominant pole of the PGA substage. To realize the necessary 2 dB gain steps, R_F is divided into 4 smaller parts whose values are tabulated in Table 16. Furthermore, the switch resistances are optimized to have adequate gain-step matching with sufficient linearity.

Table 16: Values of the Segments of the Feedback Resistor R_F

Component	**Value - Ω**
R_{20dB}	2.1 K
R_{18dB}	1.6 K
R_{16dB}	1.3 K
R_{14dB}	5 K
R_{Total}	10 K

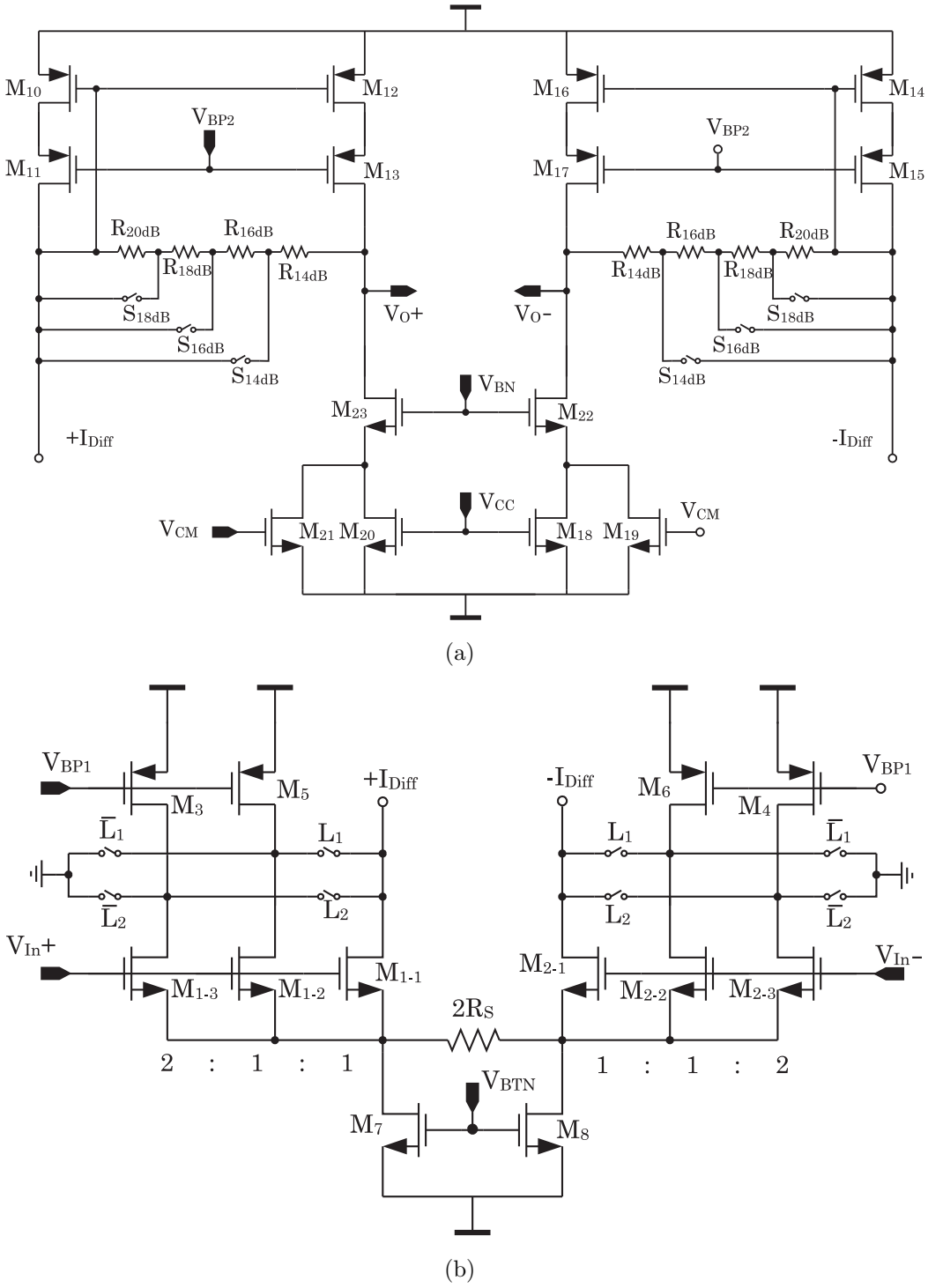


Figure 86: Schematic of the PGA. (a) The current amplifier. (b) Input transconductor.

7.3.2 Linearity

The linearity of the PGA sub-stage is dominated by the linearity of the voltage to current conversion at the input, i.e. the OTA. The SFDR of the input OTA is determined by HD3, which is given by Equation 2. The SFDR of the OTA has to be larger than 60 dB to have an better than 60 dB overall linearity. This SFDR value has to be satisfied even at the worst operation condition, for which the gain setting is 2 dB. Under this condition, the second PGA sub-stage has to handle 400 mV_P differential input voltage. This operating condition limits the overdrives of the input transistors as well as the tail-current-source transistors. For an input CM voltage of about mid-range between the supply rails, the overdrives of the input transistors should be limited to about 150 mV, which leaves only about 100 mV overdrive for the tail-current-source transistors. Using this information, the loop gain (T) can be calculated as follows:

$$\begin{aligned} \mathrm{HD_3} &= \frac{1}{32}\frac{1}{(1+\mathrm{T})^3}\left(\frac{\mathrm{V_{In}}}{\mathrm{V_{OD}}}\right)^2 \\ &= \frac{1}{32}\frac{1}{(1+\mathrm{T})^3}\left(\frac{0.4}{0.15}\right)^2 < \frac{1}{1000} \Rightarrow \mathrm{T} > 5 \Rightarrow \mathrm{T} = 6. \end{aligned} \tag{65}$$

Note that, this discussion assumes that the OTA is driving a low-impedance node such that the nonlinearity of the output impedance does not cause significant current distortion. This assumption is, in fact, valid because the OTA is driving the current mirror at the input of the current amplifier. The sensitivity of the gain of the PGA sub-stage is given by

$$\frac{\sigma^2(\Delta A)}{A^2} = \frac{\sigma^2(\Delta n)}{n^2(n+1)^2} + \frac{\sigma^2(\Delta R_F)}{R_F^2} + \frac{\sigma^2(\Delta R_S)}{R_S^2} + \frac{1}{gm_1^2(1+gm_1R_S)^2}\sigma^2(\Delta gm_1), \tag{66}$$

where A is the gain of the PGA sub-stage, n is the gain (i.e. the mirroring ratio) of the current amplifier shown in Figure 86(a), R_F is the value of the feedback resistor, gm_1 is the transconductance of M_1, and R_S is the value of the source degeneration resistance. Finally, the input-referred noise of the PGA sub-stage is given by

$$V_{In}^2 = 2\left[V_{n1}^2 + V_{n3}^2\frac{gm_3^2}{G_M^2} + V_{n5}^2\frac{gm_5^2}{G_M^2} + (R_S gm_7)^2 V_{n7}^2 + V_{n10}^2\frac{gm_{10}^2}{G_M^2} + \frac{1}{n^2}\left(V_{n12}^2\frac{gm_{12}^2}{G_M^2} + V_{n20}^2\frac{gm_{20}^2}{G_M^2} + V_{n21}^2\frac{gm_{21}^2}{G_M^2}\right)\right], \tag{67}$$

where G_M is the effective transconductance of the input OTA, which is $\frac{gm_1}{1+gm_1R_S}$.

7.3.3 Simulation Results

Several relevant simulation results showing the performance of the PGA are provided in this section. The frequency response at each gain setting, and HD3 and HD2 versus total gain are given in Figures 88 and 87 respectively.

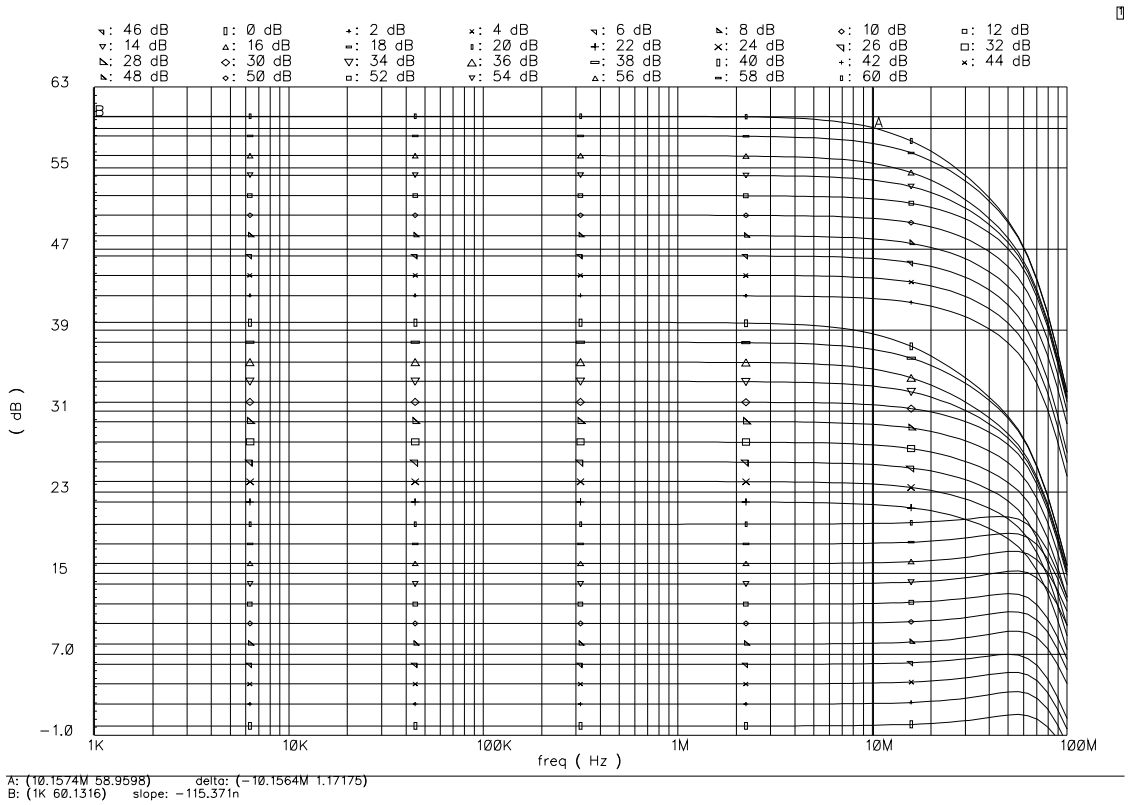


Figure 87: Frequency response of the PGA at each gain setting.

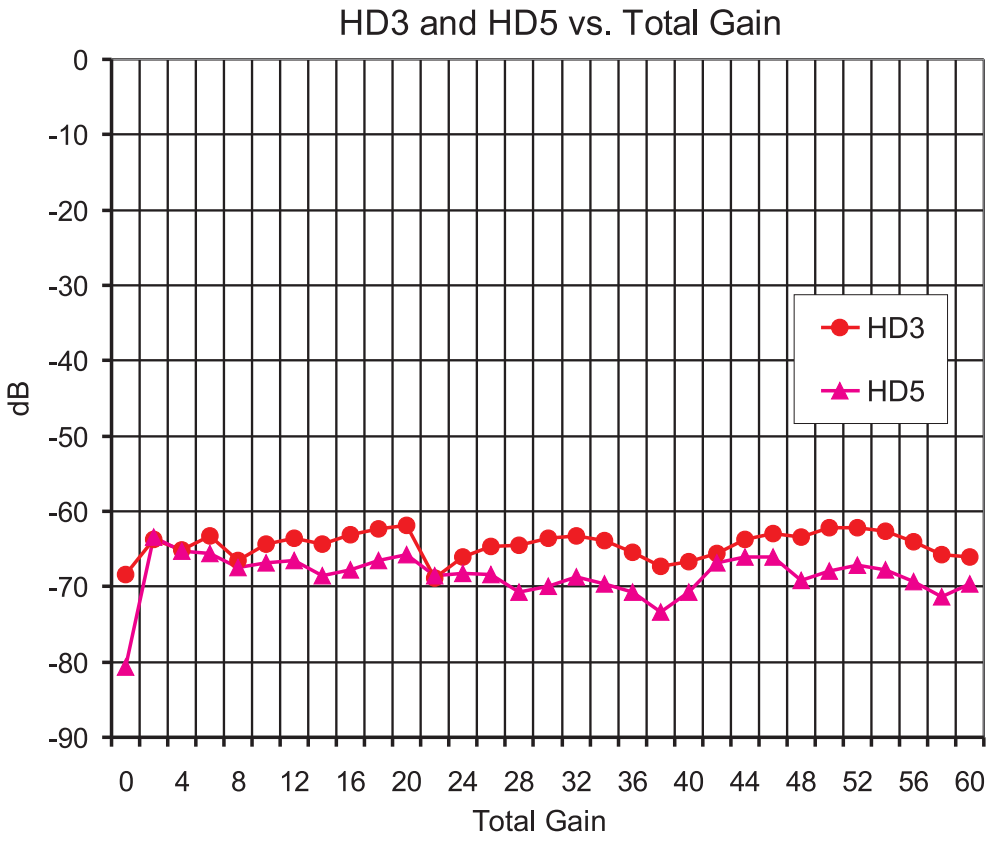


Figure 88: Output harmonics of the PGA: The third and second harmonic versus total PGA gain.

7.4 Summary

The design details of a high-dynamic-range PGA are discussed. The PGA uses an LNA stage with 20 dB fixed gain to improve SNR when the input level is low. The gain programmability is achieved by 2 current-feedback PGA sub-stages whose gain can be programmed from 2 dB to 20 dB in 2 dB steps. Even though the current-feedback PGA sub-stages can result in high bandwidths, their high-bandwidth capability is not exploited as the required BW was only 20 MHz. The proposed signal routing scheme alleviates the noise requirement on the PGA sub-stages and linearity requirement on the LNA. Therefore, it results in power and area savings. More power could be saved if the by-passed stages were shut down or their bias currents were significantly reduced from their quiescent values. A summary of the performance of the PGA is given in Table 17.

Table 17: Summary of the Simulated PGA Design Parameters

Parameter	**Condition**	**Value**
Process	CMOS	0.18μm
Supply	-	1.8V
Bias Current	LNA	4.2 mA
	PGA Sub-stage	2.5 mA
	Buffer	0.68 mA
Bandwidth	-1 dB	$\geq$ 10 MHz
	-3 dB	$\geq$ 20 MHz
Gain Step	$0-60$ dB range	2 dB
SFDR	1 V_{PP}, Over the entire gain range	$>$ 60 dB
Input-Referred Noise	LNA	$3.98\mu V_{RMS}$
	PGA Sub-stage	$57.60\mu V_{RMS}$
	Buffer	$74.14\mu V_{RMS}$
Output Load	-	5 pF

CHAPTER VIII

CONCLUSION

The CMOS technology has become the dominant process technology in today's semiconductor industry - thanks to the revolution of the digital CMOS design. However, as the channel lengths of the MOS transistors reduce with the introduction of each CMOS process node, the intrinsic gain (gm $\times$ rds) of the MOS transistors reduce. As this trend continues, the high-gain amplifiers required for accurate residue amplification in pipelined ADCs will not have sufficient gain to meet the desired specifications. Obviously, new circuit architectures and clever use of the readily available powerful DSP capability need to be exploited to decouple the gain, accuracy, and speed requirements [36].

The main objective of this research was to develop a calibration technique that would enable the design of a 2-stage pipelined ADC with an open-loop residue amplifier. This technique and its variations can potentially eliminate the need for high-gain amplifiers in pipelined ADCs, which is especially vital for the high-performance ADC design in modern fine-line CMOS technologies.

8.1 Contributions

The following sections summarize the impact of the proposed calibration ideas presented in this thesis along with the developed high-speed circuit design techniques.

8.1.1 The Double-Switching CMOS SHA

A power-efficient double-switching, switched-buffer SHA architecture was proposed and implemented. The results of this research was published in JSSC, [48]. In the hold mode, the proposed architecture has two levels of isolation from the input, which resulted in excellent hold-mode isolation. The desired linearity could be sustained with input frequencies as high as the the Nyquist rate; therefore, the usable signal BW is maximized.

The proposed double-switching architecture resulted in significant power and area savings compared to the architecture reported in [47]. The SHA architecture proposed in this research was replicated in a bipolar process by [51].

8.1.2 The Two-Step Pipelined ADC with Open-Loop Residue Amplifier

A calibration technique was developed to relax the gain-accuracy requirements in residue amplifiers. The accuracy (DC gain) and speed requirements of the residue amplifiers are decoupled. The absolute value of the interstage gain does not impact the operation of the ADC.

The calibration technique was implemented purely in the analog domain. However, the same method can be realized in the digital domain. Even though the proposed method was tailored for the current-mode techniques used throughout the design, the developed ideas can be easily implemented in switched capacitor designs. In

fact, a similar method tailored for switched-capacitor implementations was patented by [42], while the prototype ADC chip was at its layout stage.

Linear interstage-gain correction was implemented in the designed ADC. However, the proposed ideas can be extended to correct the nonlinearities in the interstage gain. The nonlinearity estimation can be done in a piece-wise linear or polynomial fashion. Correcting the nonlinearity of the interstage amplifier not only simplifies the design of the interstage amplifier but also alleviates its linearity requirements. Therefore, higher resolution and faster ADCs can be designed with simple and less noisy building blocks if the nonlinearity of the interstage amplifier is compensated.

A simple nonlinearity correction method implemented purely in an analog fashion is presented in Section 5.2.6.1. Other nonlinearity compensation methods reported in literature are [39] and [33]. The variety of the recent research on linear and nonlinear gain-error correction indicate the significance of eliminating the need for high-gain amplifiers in pipelined ADCs.

Moreover, incomplete settling in an interstage amplifier can be treated as gain errors. Therefore, the gain error correction techniques can potentially compensate settling errors [27, 39, 82].

8.1.3 The Low-Distortion PGA

Dynamic-range of a PGA is optimized by optimum use of gain stages. A signal-routing scheme is proposed. The proposed scheme allowed the optimization of PGA's linearity and SNR by by-passing unused gain stages. Consequently, the dynamic range of the PGA was maximized without dissipating excessive power.

The PGA sub-stages used in the PGA were implemented with current amplifiers, which have differential current inputs. To the best of our knowledge, the concept of current feedback is applied to this kind of current-feedback amplifiers for the first time. The results of this work is published in ISCAS05, [78].

The condition for the well-known decoupling of DC gain and BW in current amplifiers was investigated. It is shown that, the pole at the output node of the current-feedback amplifier has to be the non-dominant pole of the system to decouple the DC gain from the BW. That means, this condition necessitates a buffered output node. However, since the intended application did not require high BW, the designed current-feedback amplifiers don't have buffered outputs, which saved power and area.

8.1.4 The Slew-Rate-Boosted Pre-Charge Amplifier

A positive-feedback slew-rate-boosting technique was proposed. The proposed slew-rate-boosting technique was implemented in a pre-charge amplifier. The results of this work is published in ISCAS06, [76]. The proposed slew-rate-boosting technique demonstrates the use of positive feedback, which is controlled by a negative feedback loop. The circuit does not exhibit significant overshoot because slewing condition is sensed at its source by comparing the currents generated by the input differential pair.

The main contributions of this research are summarized in Table 18.

Table 18: Contributions

No	Description
	System-Level Contributions
1	***Proposed and designed a power-efficient double-switching switched-buffer SHA technique*, [48]** – Double switching results in exceptional hold-mode isolation and eliminates any coupling from the input – The aimed SFDR performance can be sustained with input frequencies, at least, as high as the Nyquist rate
2	***Proposed and implemented a background calibration technique for pipelined ADCs*** – The back-end reference tracks the variation in the interstage gain – Absolute value of the interstage gain is not critical – Relaxing the accuracy requirement of interstage gain is vital in fine-line CMOS processes – Relaxing the accuracy requirement of interstage gain simplifies the design of the interstage amplifier, saves power and increases speed – Interstage amplifier can be an open-loop amplifier
3	***Optimized the dynamic-range of a PGA by optimum use of gain stages*, [78]** – Total gain is achieved by cascade connection of 3 gain stages – A signal routing scheme is proposed, which allows efficient optimization of noise and linearity by by-passing unnecessary gain stages
4	***Proposed and designed a positive-feedback slew-boosting technique*, [76]**
	Circuit-Level Contributions
1	***Designed a high-speed double-switching switched-buffer CMOS SHA***
2	***Designed a high-speed two-step ADC with an open-loop residue amplifier***
3	***Proposed a mode-switching residue amplifier*** – Residue amplifier is reset by switching it from differential mode to common mode
4	***Proposed a current-input current-feedback amplifier*** – Proposed current-feedback amplifier has two low-impedance current inputs as opposed to the current-feedback amplifiers found in literature, which have one current and one voltage input
5	***Proposed a slew-rate-boosted pre-charge buffer for switched capacitor sensor interfaces***

8.2 Recommendations

- The proposed calibration method is realized purely in the analog domain, which made the implementation more cumbersome and susceptible to device parameters, coupling, etc. More sophisticated, however similar, methods can be implemented in the digital domain with better accuracy, and immunity to noise and coupling.

- The calibration methods explained in this thesis and literature depend on injecting calibration signals into the signal path and/or measuring the signal while it is processed. These processes can load the system and degrade SNR or introduce coupling, which manifests itself as spurious tones in the output spectrum, see Figure 61. Therefore, calibration signals must be injected into the signal stream with utmost care. Randomizing the injected signal or injection sequence can eliminate periodicity and smear the spurious tones caused by the calibration into the noise floor.

- Nonlinear gain calibration is a powerful method to relax not only the gain but also the linearity requirements in the interstage amplifiers. If nonlinear calibration is implemented, the interstage amplifier can be an open-loop circuit even in very high-resolution pipelined ADCs.

- Incomplete settling in an interstage amplifier can be treated as gain error. The gain error calibration techniques can be used to compensate settling errors, which can improve speed, and reduce power and design complexity.

- In modern fine-line CMOS processes, the achievable open-loop gains can limit the resolution in pipelined ADCs. Therefore, some sort of calibration must be used to alleviate the gain-accuracy and linearity requirements in the interstage amplifiers (MDACs.) With the use of clever calibration techniques, higher resolution and faster ADCs can be designed with simple and less noisy analog building blocks.

- Analog circuit design in fine-line CMOS processes must take full advantage of the readily available DSP power through the use of clever digital calibration techniques.

- Since current switching is more natural in bipolar technologies, the proposed double-switching switched-buffer SHA technique is more suitable for bipolar technologies. Further, the linearization methods proposed by [66, 83] can be used to linearize the blocks used in the SHA.

8.3 The Future

Most of the techniques and circuit topologies that constitute the design arsenal of analog designers in older CMOS processes are not useful or practical in deep-sub-micron CMOS processes. The design objective in deep-sub-micron CMOS processes must be to achieve high signal-processing accuracy by assisting the analog circuitry with DSP while minimizing the complexity of the analog circuitry, [36]. The future challenge of the analog designer is to come up with efficient calibration techniques that result in minimal analog complexity.

APPENDIX A

LIST OF ANALOG-TO-DIGITAL CONVERTERS

Technology nomenclature: Number: CMOS process with minimum channel length of "number" μm.

Number BiCMOS: Silicon BiCMOS process with minimum channel length of "number" μm.

Number SiGe: Silicon-Germanium BiCMOS process with minimum channel length of "number" μm.

Number Bipolar: Bipolar process with minimum base width of "number" μm.

Number C-Bipolar: Complementary bipolar process with minimum base width of "number" μm.

Conversion Rate: For Nyquist-rate converters, conversion rate is equal to the sampling rate. For over-sampling converters the number written under conversion rate corresponds to signal bandwidth.

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
40000	4	-	-	-	0.13 SiGe	Interleaved	JSSC	2010
2700	6	50	1	0.8	90nm	Folding	JSSC	2010
2200	6	2.6	1.1	0.68	40nm	Int-Pipelined	JSSC	2010
1000	6	6.7	1.2	1	65nm	Int-SAR	JSSC	2010
250	16	1	1.8/3	2.5	0.18	Pipelined	JSSC	2010
160	11	594	3.3	1.8	0.35	Int-Pipelined	JSSC	2010
160	16	1630	5/3.3	2.5	0.25 C-BiCMOS	Pipelined	JSSC	2010
100	10	3	1.2	1.2	90nm	SAR	JSSC	2010
100	10	6	1	1	90nm	Two_Step	JSSC	2010
50	10	0.826	1.2	2	0.13	SAR	JSSC	2010
50	10	9.9	1.8	1	0.18	Pipelined	JSSC	2010
42	10	11.1	1.8	1.8	0.18	Pipelined	JSSC	2010
26	11	26.7	1.8	3.6	0.18	Pipelined	JSSC	2010
25	11	48	1.8	-	0.18	Σ-Δ	JSSC	2010
20	11	17.2	1.8	1.4	0.18	Pipelined	JSSC	2010
18	10	183	1.8	1	0.18	Σ-Δ	JSSC	2010
18	12	17	2.5/1.2	0.8	65nm	Σ-Δ	JSSC	2010
12.5	18	105	2.5/5	-	0.25	Pipe. SAR	JSSC	2010
10	11	5.32	1.1	-	0.13	Σ-Δ	JSSC	2010
10	12	160	1.8	0.5	0.18	Σ-Δ	JSSC	2010
10	11	6.8	1.2	1.9	90nm	Σ-Δ	JSSC	2010
6.7	12	36	1.8	1.8	0.18	Σ-Δ	JSSC	2010
1.92	10	3.1	1.2	0.6	0.13	Σ-Δ	JSSC	2010
1	15	38.1	1.8	-	0.18	Σ-Δ-SAR	JSSC	2010
35000	4	4500	3.3	0.24	0.18 SiGe	Flash	JSSC	2009
4800	5	300	1.2	0.5	0.13	Interleaved	JSSC	2009
1750	5	2.2	1	0.8	90nm	Folding	JSSC	2009
1600	6	49	1.2	1	0.13	Two-Step	JSSC	2009
1250	6	32	1.2	1,2	0.13	SAR	JSSC	2009
1000	6	650	2.5	-	0.13 SiGe	Σ-Δ	JSSC	2009
1000	10	1200	1.8	0.82	0.18	Folding	JSSC	2009
800	6	12	1.2	-	65nm	Flash	JSSC	2009
770	8	70	1.2	1.4	90nm	Subranging	JSSC	2009
500	10	55	1.2	1.2	90nm	Pipelined	JSSC	2009
200	12	348	1.2	1.2	90nm	Pipelined	JSSC	2009
125	16	385	1.8	2	0.18	Pipelined	JSSC	2009
100	14	250	1.2	1.6	90nm	Pipelined	JSSC	2009
100	14	130	1.2	1.5	90nm	Pipelined	JSSC	2009
80	11	36	1.8	1.6	0.18	Pipelined	JSSC	2009
60	15	300	1.8	2.4	0.18	Pipelined	JSSC	2009

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
40000	4	-	-	-	0.13 SiGe	Interleaved	JSSC	2010
2700	6	50	1	0.8	90nm	Folding	JSSC	2010
2200	6	2.6	1.1	0.68	40nm	Int-Pipelined	JSSC	2010
1000	6	6.7	1.2	1	65nm	Int-SAR	JSSC	2010
250	16	1	1.8/3	2.5	0.18	Pipelined	JSSC	2010
160	11	594	3.3	1.8	0.35	Int-Pipelined	JSSC	2010
160	16	1630	5/3.3	2.5	0.25 C-BiCMOS	Pipelined	JSSC	2010
100	10	3	1.2	1.2	90nm	SAR	JSSC	2010
100	10	6	1	1	90nm	Two_Step	JSSC	2010
50	10	0.826	1.2	2	0.13	SAR	JSSC	2010
50	10	9.9	1.8	1	0.18	Pipelined	JSSC	2010
42	10	11.1	1.8	1.8	0.18	Pipelined	JSSC	2010
26	11	26.7	1.8	3.6	0.18	Pipelined	JSSC	2010
25	11	48	1.8	-	0.18	Σ-Δ	JSSC	2010
20	11	17.2	1.8	1.4	0.18	Pipelined	JSSC	2010
18	10	183	1.8	1	0.18	Σ-Δ	JSSC	2010
18	12	17	2.5/1.2	0.8	65nm	Σ-Δ	JSSC	2010
12.5	18	105	2.5/5	-	0.25	Pipe. SAR	JSSC	2010
10	11	5.32	1.1	-	0.13	Σ-Δ	JSSC	2010
10	12	160	1.8	0.5	0.18	Σ-Δ	JSSC	2010
10	11	6.8	1.2	1.9	90nm	Σ-Δ	JSSC	2010
6.7	12	36	1.8	1.8	0.18	Σ-Δ	JSSC	2010
1.92	10	3.1	1.2	0.6	0.13	Σ-Δ	JSSC	2010
1	15	38.1	1.8	-	0.18	Σ-Δ-SAR	JSSC	2010
35000	4	4500	3.3	0.24	0.18 SiGe	Flash	JSSC	2009
4800	5	300	1.2	0.5	0.13	Interleaved	JSSC	2009
1750	5	2.2	1	0.8	90nm	Folding	JSSC	2009
1600	6	49	1.2	1	0.13	Two-Step	JSSC	2009
1250	6	32	1.2	1,2	0.13	SAR	JSSC	2009
1000	6	650	2.5	-	0.13 SiGe	Σ-Δ	JSSC	2009
1000	10	1200	1.8	0.82	0.18	Folding	JSSC	2009
800	6	12	1.2	-	65nm	Flash	JSSC	2009
770	8	70	1.2	1.4	90nm	Subranging	JSSC	2009
500	10	55	1.2	1.2	90nm	Pipelined	JSSC	2009
200	12	348	1.2	1.2	90nm	Pipelined	JSSC	2009
125	16	385	1.8	2	0.18	Pipelined	JSSC	2009
100	14	250	1.2	1.6	90nm	Pipelined	JSSC	2009
100	14	130	1.2	1.5	90nm	Pipelined	JSSC	2009
80	11	36	1.8	1.6	0.18	Pipelined	JSSC	2009
60	15	300	1.8	2.4	0.18	Pipelined	JSSC	2009

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
4000	4	7.8	1.8/2.5	0.92	0.18	Flash	JSSC	2007
800	11	350	1.5	1	0.09	Interleaved	ISSCC	2007
800	6	105	1.8	0.4	0.18	Pipelined	JSSC	2007
500	5	7.8	1.2	0.8	0.18	SAR	JSSC	2007
205	10	61	1	1	0.09	Pipelined	ISSCC	2007
205	10	92.5	1.2-3.3	1	0.13	Pipelined	ISSCC	2007
205	10	40	1	1	0.09	Pipelined	JSSC	2007
200	8	8.5	1.8	1	0.18	Pipelined	ISSCC	2007
200	8	8.5	1.8	2	0.18	Pipelined	JSSC	2007
160	10	64	1	N/A	0.09	Subrangimg	ISSCC	2007
125	15	909	1.8	1.4	0.18	Pipelined	JSSC	2007
100	8	30	1	0.5	0.18	Pipelined	JSSC	2007
100	10	33	1	0.8	0.09	Pipelined	JSSC	2007
80	10	6.5	0.8	1.2	0.09	Pipelined	ISSCC	2007
75	12	273	3	2	0.35	Pipelined	JSSC	2007
50	10	18	1.8	1	0.18	Pipelined	JSSC	2007
40	14	66	1.5	1.8	0.13	SAR	ISSCC	2007
40	13	268	1.8	1.6	0.18	Pipelined	JSSC	2007
30	10	4.7	1	1	0.09	Pipelined	ISSCC	2007
20	8	0.29	1	N/A	0.09	SAR	ISSCC	2007
20	11.5	56	1.2	1	0.09	Σ-Δ	JSSC	2007
10	10	20.5	1.2	N/A	0.13	Σ-Δ	ISSCC	2007
2.5	14	50	2.5	N/A	0.25	Σ-Δ	JSSC	2007
2.2	14	180	2.5	N/A	0.25	Σ-Δ	JSSC	2007
1.5	6	0.007	0.5	1	0.09	SAR	JSSC	2007
1.25	14	14	2.4	2	0.25	Σ-Δ	JSSC	2007
1.1	12.5	5.4	1.8	1.6	0.18	Σ-Δ	JSSC	2007
1	9	75	2.5	N/A	0.25 BiCMOS	Σ-Δ	JSSC	2007
0.2	8	0.0025	1	1	0.18	SAR	JSSC	2007
0.1	12	0.025	1	2	0.18	SAR	JSSC	2007
22000	5	3000	3.3	1.3	0.13 BiCMOS	Flash	ISSCC	2006
6000	4	780	1.8	0.4	0.18	Pipelined	JSSC	2006
1000	11	250	1.2	N/A	0.13	Interleaved	JSSC	2006
600	6	5.3	1.2	N/A	0.13	AS	ISSCC	2006
600	5	70	1.8	0.4	0.18	Pipelined	JSSC	2006
400	10	160	1.2	1.2	0.13	Pipelined	JSSC	2006
180	13	736	3.3	1.4	0.25	Pipelined	JSSC	2006
160	6	50	3.3	3.4	0.35	Flash	JSSC	2006
125	14	1000	3.3	2	0.35 BiCMOS	Pipelined	JSSC	2006
100	14	224	1.5	1.5	0.13	Pipelined	ISSCC	2006

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
100	10	35	1.2	0.8	0.09	Pipelined	ISSCC	2006
100	10	55	1.2	0.8	0.09	Pipelined	JSSC	2006
80	14	1200	3.3/5	2	0.35 BiCMOS	Pipelined	JSSC	2006
50	10	15	1.2/2.7	2	0.13	Pipelined	ISSCC	2006
50	12	18	1.8	1	0.18	Pipelined	ISSCC	2006
44	10	20	2.5	3	0.25 BiCMOS	Pipelined	JSSC	2006
40	13	268	1.8	1.6	0.18	Pipelined	ISSCC	2006
40	12	30	0.7/1.6	1.5	0.09	Subranging	ISSCC	2006
40	11	73	2.8	2.4	0.18	Pipelined	JSSC	2006
30	15	145	3.3	N/A	0.18	Subranging	JSSC	2006
20	12	70	1.2	N/A	0.13	Σ-Δ	ISSCC	2006
20	9	32	2.5	0.35	0.25	Σ-Δ	JSSC	2006
20	9	103	1.8	0.8	0.18	Σ-Δ	JSSC	2006
20	14	35	2.8	N/A	0.18	Pipelined	JSSC	2006
20	12	20	1.2	1.6	0.13	Σ-Δ	JSSC	2006
8.5	11.5	375	1.8	1.8	0.18	Σ-Δ	ISSCC	2006
8.5	13	375	3.3	N/A	0.18	Σ-Δ	JSSC	2006
4	11.5	35	1.8	1.5	0.18	Σ-Δ	ISSCC	2006
0.1	12	0.025	1	N/A	0.18	SAR	ISSCC	2006
2000	6	310	1.8	1	0.18	Flash	JSSC	2005
1200	6	160	1.5	1	0.13	Flash	JSSC	2005
200	8	10	1.8	1	0.18	Pipelined	ISSCC	2005
200	8	30	1.8	1	0.18	Pipelined	ISSCC	2005
150	8	71	1.8	1.6	0.18	Pipeline	JSSC	2005
125	10	40	1.8	N/A	0.18	Pipelined	ISSCC	2005
110	12	97	1.8	2	0.18	Pipelined	JSSC	2005
80	12	755	2.5	0.5	2.5	Pipeline	JSSC	2005
65	16	970	3.3	4	0.4 SiGe	Pipeline	JSSC	2005
50	10	35	1.8	1.2	0.18	Pipelined	ISSCC	2005
50	10	35	1.8	1.6	0.18	Pipelined	JSSC	2005
40	15	370	2.5	2	2.5	Pipeline	JSSC	2005
23	11	42.6	1.8	1.5	0.18	Σ-Δ	ISSCC	2005
20	12	240	3.3	2	0.18	Σ-Δ	ISSCC	2005
12	10	3.3	1.2	1	0.09	Pipelined	ISSCC	2005
5	12	12	0.9	0.9	0.18	Pipeline	JSSC	2005
2	6	2.1	1.3	1.6	0.13	Σ-Δ	ISSCC	2005
2	11	3	1.5	1.2	0.13	Σ-Δ	ISSCC	2005
2	10	1.2	1.2	1.5	0.09	Σ-Δ	ISSCC	2005
2	12	3	1.5	1.2	0.13	Σ-Δ	JSSC	2005
1.25	15	87	1.2/2.5	1.2	0.13	Σ-Δ	JSSC	2005

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
1	16	105	2.5	N/A	0.25	Pipelined	ISSCC	2005
1	16	215	2.5/5	6.56	0.25	Σ-Δ	ISSCC	2005
1	14	4.7	1.8	N/A	0.18	Σ-Δ	ISSCC	2005
1	16	105	2.5	N/A	0.25	Pipelined	JSSC	2005
0.615	14	5.4	1.2	N/A	0.09	Σ-Δ	ISSCC	2005
0.5	12	2.1	1.3	0.8	0.09	Σ-Δ	JSSC	2005
0.024	12	1	0.6	0.8	0.35	Σ-Δ	ISSCC	2005
0.024	13	1	0.6	0.8	0.35	Σ-Δ	JSSC	2005
0.02	17.6	18	3.3	2.8	0.35	Σ-Δ	ISSCC	2005
0.02	17	32	3.3	2.8	0.35	Σ-Δ	JSSC	2005
40000	3	3800	.	.	0.12 SiGe	Flash	ISSCC	2004
10000	5	3600	3.7	1	0.18 BiCMOS	Flash	JSSC	2004
2000	8	3500	3	.	BiCMOS	Folding	JSSC	2004
1600	8	902	1.8	0.8	0.18	Folding	ISSCC	2004
600	8	200	3.3	.	0.18	Folding	ISSCC	2004
600	6	10	1.2	.	0.09	Interleaved	ISSCC	2004
220	10	135	1.2	1	0.13	Pipelined	ISSCC	2004
150	8	71	1.8	1.6	0.18	Pipelined	ISSCC	2004
150	10	123	1.8	1	0.18	Pipelined	JSSC	2004
125	8	21	1.2	.	0.13	Subranging	ISSCC	2004
100	10	67	1.8	.	0.18	Pipelined	JSSC	2004
80	12	.	2.5	1	0.25	Pipelined	ISSCC	2004
80	10	33	1.5	.	0.13	Pipelined	ISSCC	2004
50	12	780	2.5	1.2	0.25	Pipelined	ISSCC	2004
50	14	350	3	.	0.18	Pipelined	ISSCC	2004
40	15	400	1.8	2.25	0.18	Pipelined	ISSCC	2004
40	10	12	2.5	.	0.25	Pipelined	JSSC	2004
20	15	215	3.3	1.4	0.18	Pipelined	ISSCC	2004
20	12	254	3.3	1.6	0.35	Pipelined	JSSC	2004
16	13	78	1.3	1.3	0.25	Pipelined	JSSC	2004
15	11	70	1.5	1.2	0.13	Σ-Δ	JSSC	2004
12.5	14	200	1.8	1.6	0.18	Σ-Δ	ISSCC	2004
12	14	112	1.8	2	0.18	Pipelined	ISSCC	2004
10	11	122.4	1.8	0.565	0.18	Σ-Δ	ISSCC	2004
2.5	12	150	1.4	.	0.18	Σ-Δ	ISSCC	2004
2	14	149	1.8	.	1.8	Σ-Δ	JSSC	2004
1.9	8	1.5	0.9	0.75	0.13	Σ-Δ	ISSCC	2004
1.1	13	8	1.5	.	0.13	Σ-Δ	ISSCC	2004
1.1	14	62	3.3	2.4	0.5	Σ-Δ	JSSC	2004
1	12.5	6	1.8	1	0.18	Σ-Δ	ISSCC	2004

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
1	14.5	2	.	.	0.18	Σ-Δ	ISSCC	2004
0.5	13.5	58	3.3	2.6	0.6	Σ-Δ	JSSC	2004
0.02	13.5	0.13	1	0.6	0.09	Σ-Δ	ISSCC	2004
250	6	30	0.8-3.3	R-R	0.35	SAR	JSSC	2003
200	8	655	3.3	1.3	0.35	Interpol.	JSSC	2003
46	12.5	50	2.7	2.4	0.18	Σ-Δ	JSSC	2003
30	10	16	2	1.6	0.3	Pipelined	JSSC	2003
20	8	25.4	3	1	0.35	Pipeline	JSSC	2003
0.048	17	230	3.3	2	0.35	Σ-Δ	JSSC	2003
1600	6	328	1.95	N/A	0.18	Flash	JSSC	2002
450	6	50	1.8	0.8	0.18	Flash	ISSCC	2002
400	6	150	2.5	N/A	0.25	Flash	JSSC	2002
400	6	150	2-2.8	N/A	0.25	Flash	JSSC	2002
120	10	234	3.3	3	0.35	Interleaved	ISSCC	2002
120	10	234	3.3	3	0.35	Interleaved	JSSC	2002
61	12	600	3.4	1.4	0.35	Pipelined	JSSC	2002
40	9	425	N/A	N/A	0.25	Pipelined	TSC-II	2002
30	10	16	2	1.6	0.3	Pipelined	ISSCC	2002
25	6	0.48	1	0.64	0.13	Flash	JSSC	2002
20	10	12	1.2	N/A	0.13	SAR	ISSCC	2002
10	14	220	5	4	0.5	Pipelined	JSSC	2002
2	12	105	2.5	N/A	0.25	Σ-Δ	JSSC	2002
1.1	14	230	3.3	2.4	1.8	Σ-Δ	JSSC	2002
0.5	12	12	2.7	1.3	0.35 BiCMOS	Σ-Δ	JSSC	2002
0.33	13	50	2.7	N/A	0.35 BiCMOS	Σ-Δ	JSSC	2002
0.27	12	56	3	N/A	0.35	Σ-Δ	JSSC	2002
0.25	12	77	2.5	2	0.25	Σ-Δ	JSSC	2002
0.2	7	12	1	N/A	0.35	Σ-Δ	JSSC	2002
0.18	13.5	5	1.8-2.4	0.7	0.35 BiCMOS	Σ-Δ	JSSC	2002
0.02	12	5.6	1	1.2	0.35	Σ-Δ	JSSC	2002
0.011	10	1.7	1.8	0.125	0.5	Σ-Δ	JSSC	2002
1300	6	500	3.3	1.6	0.35	Flash	JSSC	2001
1100	6	300	3.3	1.5	0.35	Flash	ISSCC	2001
100	10	180	1.8	1	0.18	Pipelined	ISSCC	2001
100	8	110	3.8-2.2	2.7	0.35	Subranging	JSSC	2001
100	8	165	5	2	0.5	Folding	JSSC	2001
80	8	268	3	1.75	0.35	Pipelined	JSSC	2001
75	14	340	3	2	0.35	Pipelined	ISSCC	2001
75	14	340	3	2	0.35	Pipelined	JSSC	2001
54	12	295	2.5	N/A	0.25	Subranging	ISSCC	2001

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
1	14.5	2	.	.	0.18	Σ-Δ	ISSCC	2004
0.5	13.5	58	3.3	2.6	0.6	Σ-Δ	JSSC	2004
0.02	13.5	0.13	1	0.6	0.09	Σ-Δ	ISSCC	2004
250	6	30	0.8-3.3	R-R	0.35	SAR	JSSC	2003
200	8	655	3.3	1.3	0.35	Interpol.	JSSC	2003
46	12.5	50	2.7	2.4	0.18	Σ-Δ	JSSC	2003
30	10	16	2	1.6	0.3	Pipelined	JSSC	2003
20	8	25.4	3	1	0.35	Pipeline	JSSC	2003
0.048	17	230	3.3	2	0.35	Σ-Δ	JSSC	2003
1600	6	328	1.95	N/A	0.18	Flash	JSSC	2002
450	6	50	1.8	0.8	0.18	Flash	ISSCC	2002
400	6	150	2.5	N/A	0.25	Flash	JSSC	2002
400	6	150	2-2.8	N/A	0.25	Flash	JSSC	2002
120	10	234	3.3	3	0.35	Interleaved	ISSCC	2002
120	10	234	3.3	3	0.35	Interleaved	JSSC	2002
61	12	600	3.4	1.4	0.35	Pipelined	JSSC	2002
40	9	425	N/A	N/A	0.25	Pipelined	TSC-II	2002
30	10	16	2	1.6	0.3	Pipelined	ISSCC	2002
25	6	0.48	1	0.64	0.13	Flash	JSSC	2002
20	10	12	1.2	N/A	0.13	SAR	ISSCC	2002
10	14	220	5	4	0.5	Pipelined	JSSC	2002
2	12	105	2.5	N/A	0.25	Σ-Δ	JSSC	2002
1.1	14	230	3.3	2.4	1.8	Σ-Δ	JSSC	2002
0.5	12	12	2.7	1.3	0.35 BiCMOS	Σ-Δ	JSSC	2002
0.33	13	50	2.7	N/A	0.35 BiCMOS	Σ-Δ	JSSC	2002
0.27	12	56	3	N/A	0.35	Σ-Δ	JSSC	2002
0.25	12	77	2.5	2	0.25	Σ-Δ	JSSC	2002
0.2	7	12	1	N/A	0.35	Σ-Δ	JSSC	2002
0.18	13.5	5	1.8-2.4	0.7	0.35 BiCMOS	Σ-Δ	JSSC	2002
0.02	12	5.6	1	1.2	0.35	Σ-Δ	JSSC	2002
0.011	10	1.7	1.8	0.125	0.5	Σ-Δ	JSSC	2002
1300	6	500	3.3	1.6	0.35	Flash	JSSC	2001
1100	6	300	3.3	1.5	0.35	Flash	ISSCC	2001
100	10	180	1.8	1	0.18	Pipelined	ISSCC	2001
100	8	110	3.8-2.2	2.7	0.35	Subranging	JSSC	2001
100	8	165	5	2	0.5	Folding	JSSC	2001
80	8	268	3	1.75	0.35	Pipelined	JSSC	2001
75	14	340	3	2	0.35	Pipelined	ISSCC	2001
75	14	340	3	2	0.35	Pipelined	JSSC	2001
54	12	295	2.5	N/A	0.25	Subranging	ISSCC	2001

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
25	10	195	3.3	1.6	0.35	Subranging	JSSC	1999
20	10	75	5	2	0.5	Subranging	ISSCC	1999
20	10	75	5	1.75	0.5	Subranging	JSSC	1999
18	13	230	5	1.5	0.6	Σ-Δ	JSSC	1999
14.3	10	36	1.5	1.6	0.6	Pipelined	JSSC	1999
3.3	12	300	5	N/A	0.5	Pipelined	TCAS	1999
1.1	15	200	3.3	N/A	0.5	Σ-Δ	JSSC	1999
1.1	12.9	55	5	4	0.7	Σ-Δ	JSSC	1999
0.8	12	1.9	3.3	0.5mA	2	Cyclic	TCAS	1999
0.2	10	157	5	3	0.8	Σ-Δ	JSSC	1999
0.125	12	16	5	4	1.5	Algorithmic	JSSC	1999
0.0004	20	16	5	2.5	0.6	Σ-Δ	JSSC	1999
400	6	200	3.2	4.6	0.5 BiCMOS	Folding	ISSCC	1998
400	6	190	3	1	CMOS	Flash	ISSCC	1998
400	6	300	3.2	2.3	0.5 BiCMOS	Folding	JSSC	1998
400	6	190	3	1	0.35	Flash	JSSC	1998
350	6	225	3.3		0.35 BiCMOS	Flash	ISSCC	1998
200	6	380	5	N/A	N/A	Flash	JSSC	1998
75	8	70	3.3	N/A	0.5	Interleaved	ISSCC	1998
40	10	650	5	4	1	Interleaved	JSSC	1998
20	12	250	5	2	0.7	Pipeline	JSSC	1998
10	12	265	3.3	N/A	0.5	Pipelined	ISSCC	1998
10	12	338	3.3	2	0.5	Pipeline	JSSC	1998
1	15	230	5	4	1	Σ-Δ	JSSC	1998
0.7	12	81	3.3	N/A	0.7	Σ-Δ	JSSC	1998
0.2	10	7	3.3	2.8	0.6	Algorithmic	JSSC	1998
0.2	10	12	5	2	1	SAR	JSSC	1998
0.1	12	9.6	2.7	N/A	0.6	Σ-Δ	JSSC	1998
0.012	10	2	1.5	0.1mA	0.8	Cyclic	JSSC	1998
100	10	1100	5	2	1	Interleaved	JSSC	1997
60	12	300	5	2	1 BiCMOS	Folding	JSSC	1997
52	8	250	5	N/A	0.9	Interleaved	JSSC	1997
50	10	240	5	2	0.5	Folding	JSSC	1997
5	15	130	5	2	1.4	Pipelined	JSSC	1997
1.25	16	550	5	4	0.6	Σ-Δ	JSSC	1997
0.025	16	2.5	1.8	3.2	0.8	Σ-Δ	JSSC	1997
0.024	24	520	5	5	0.7	Σ-Δ	JSSC	1997
0.008	12	0.62	2.5	N/A	1.2	Σ-Δ	JSSC	1997
0.005	14	340	5	N/A	0.8	Σ-Δ	JSSC	1997
0.001	14	3.6	1.5	2	0.5	Σ-Δ	JSSC	1997

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
0.0008	19	2.7	5	10	2	Σ-Δ	JSSC	1997
200	6	400	5	N/A	0.6	Flash	ISSCC	1996
200	6	110	3	1.5	0.5	Flash	JSSC	1996
175	6	160	3.3	1.2	0.7	Flash	JSSC	1996
125	8	225	5	2.5	1	Folding	JSSC	1996
80	8	80	3.3	3.2	0.5	Folding	ISSCC	1996
80	8	80	3.3	1.6	0.5	Folding	JSSC	1996
40	10	400	5	2.5	1.4 BiCMOS	Pipelined	JSSC	1996
15	8	8	1.5	0.8	0.5 BiCMOS	Interleaved	ISSCC	1996
15	8	350	5	768uA	0.8	Pipelined	JSSC	1996
10	12	250	5	2	0.8	Pipelined	ISSCC	1996
10	12	250	5	2	0.8	Pipelined	JSSC	1996
10	13	360	5	4	1.4 BiCMOS	Pipelined	JSSC	1996
5	13	166	5	6.6	1.2	Pipelined	JSSC	1996
5	12	33	2.5	1	1.2	Pipelined	JSSC	1996
2.5	14	500	10	5	2 BiCMOS	Pipelined	JSSC	1996
1	16	200	5	5	1 BiCMOS	Pipelinep	ISSCC	1996
1	12	25	5	N/A	1	Interleaved	JSSC	1996
1	16	250	5	5	1 BiCMOS	Pipelined	JSSC	1996
0.25	14	58	5	6	1.2	Σ-Δ	JSSC	1996
0.01	14	50	5	N/A	0.8	Algorithmic	JSSC	1996
0.003	13	0.2	2.2	N/A	0.5	Σ-Δ	JSSC	1996
0.0004	14	13	5	4	2	Σ-Δ	JSSC	1996
150	8	350	5	1	1 BiCMOS	Folding	ISSCC	1995
100	8	250	5	N/A	1	Folding	ISSCC	1995
70	8	110	5	2	0.8	Folding	ISSCC	1995
70	8	110	5	2	0.8	Folding	JSSC	1995
50	12	575	5	1	C-Bipolar	Subranging	ISSCC	1995
20	10	20	2	2	0.5	Subranging	ISSCC	1995
20	10	50	5	2	1.2	Pipelined	JSSC	1995
4.5	8	16	5	260uA	0.8	Pipeline	JSSC	1995
3	10	15	3	2	0.8	Cyclic	ISSCC	1995
0.05	8	0.2	5	3	2	Algorithmic	JSSC	1995
20	10	135	3	1	0.8	Subranging	ISSCC	1994
0.001	14	16x0.94	5	5	2	Σ-Δ	JSSC	1994
100	10	950	5	2	0.8 BiCMOS	Pipelined	ISSCC	1993
85	8	1100	5	3.2	1	Interleaved	JSSC	1993
32	10	500	5	2	1	Subranging	ISSCC	1993
20	10	30	2.5	2	0.8	Pipelined	ISSCC	1993
20	10	30	2.5	N/A	0.8	Pipelined	JSSC	1993

Conv. Rate MSample/s	Res. bits	Power mW	Supply V	Input V pp	Technology µm	Topology	Source	Year
13.5	8	150	5	1.5	1	Subranging	JSSC	1993
1	15	1800	+/-5	4	2.4 BiCMOS	Pipelined	ISSCC	1993
1	15	1800	8	4	2.4 BiCMOS	Pipelined	JSSC	1993
0.2	12	10	5	5	1	SAR	JSSC	1993
0.02	15	N/A	5	4	2	Σ-Δ	JSSC	1993
650	8	850	4.5	1	1 Bipolar	Folding	JSSC	1992
20	12	3500	+/-5	1.84	Bipolar	Pipelined	ISSCC	1992
20	10	240	5	N/A	0.9	Pipelined	JSSC	1992
5	12	200	5	5	1	Subranging	ISSCC	1992
5	12	200	5	5	1	Subranging	JSSC	1992
1.00E-06	20	6.7	5	N/A	2	Integrating	JSSC	1992
1000	6	2800	5.2	1	1.5 Bipolar	Interleaved	ISSCC	1991
500	8	3100	5.2	2	0.6 Bipolar	Flash	ISSCC	1991
20	10	1000	10	1	2 BiCMOS	Pipelined	JSSC	1991
1.25	12	600	10	10	2 BiCMOS	Subranging	JSSC	1991
75	10	2000	5	1	1.5 Bipolar	Subranging	ISSCC	1990
75	10	2000	10	1	1.5 Bipolar	Subranging	JSSC	1990
30	10	750	+/-5	2	1.2 BiCMOS	Folding	ISSCC	1990
20	10	1000	5/+10	1	2 BiCMOS	Pipelined	ISSCC	1990
0.001	18	120	+/-5	20	CMOS+ BiCMOS	SAR	ISSCC	1990
13.5	8	150	5	1.5	1	Subranging	JSSC	1993

APPENDIX B

BONDING DIAGRAMS

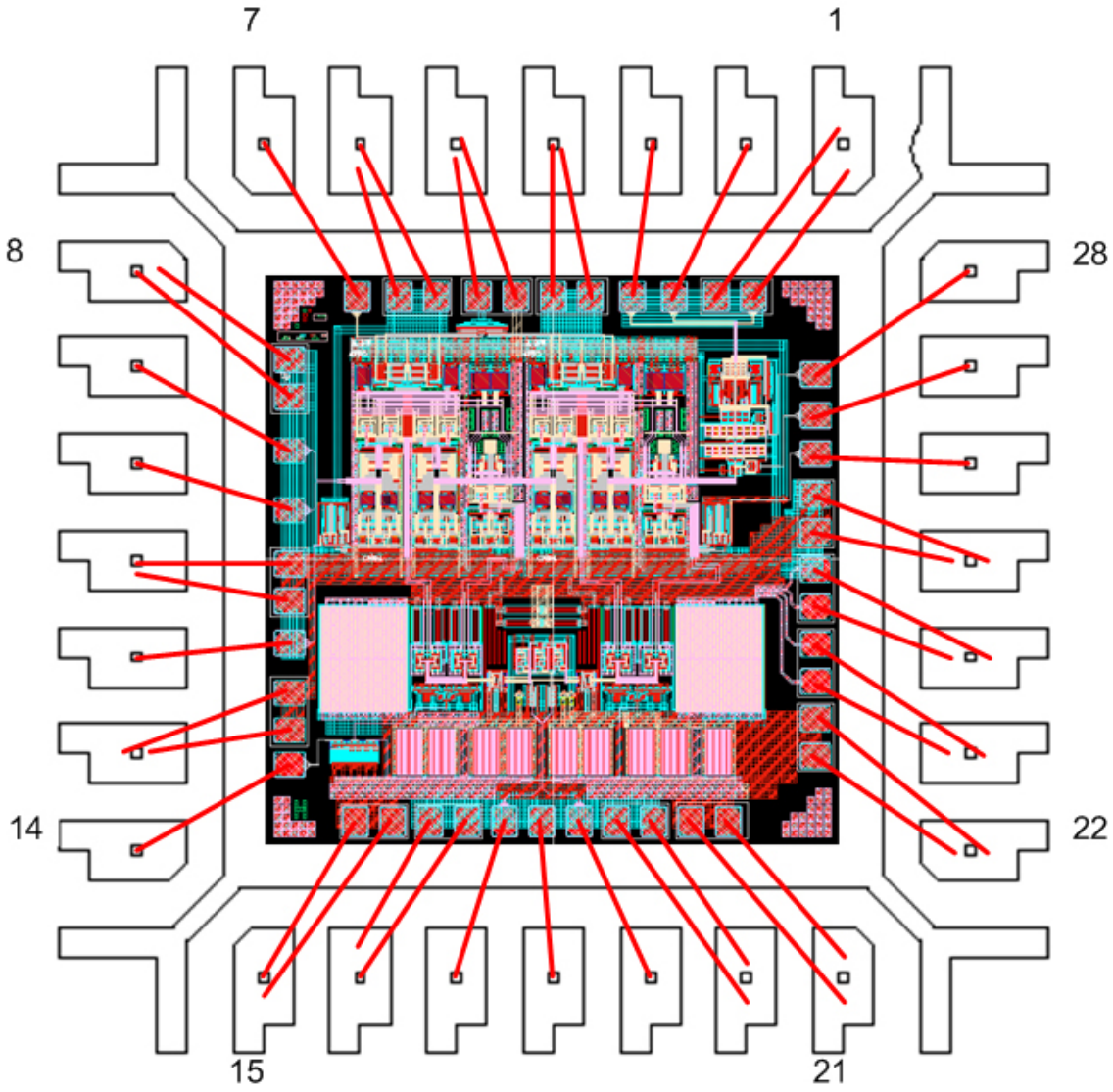


Figure 89: Bonding diagram of the first SHA chip.

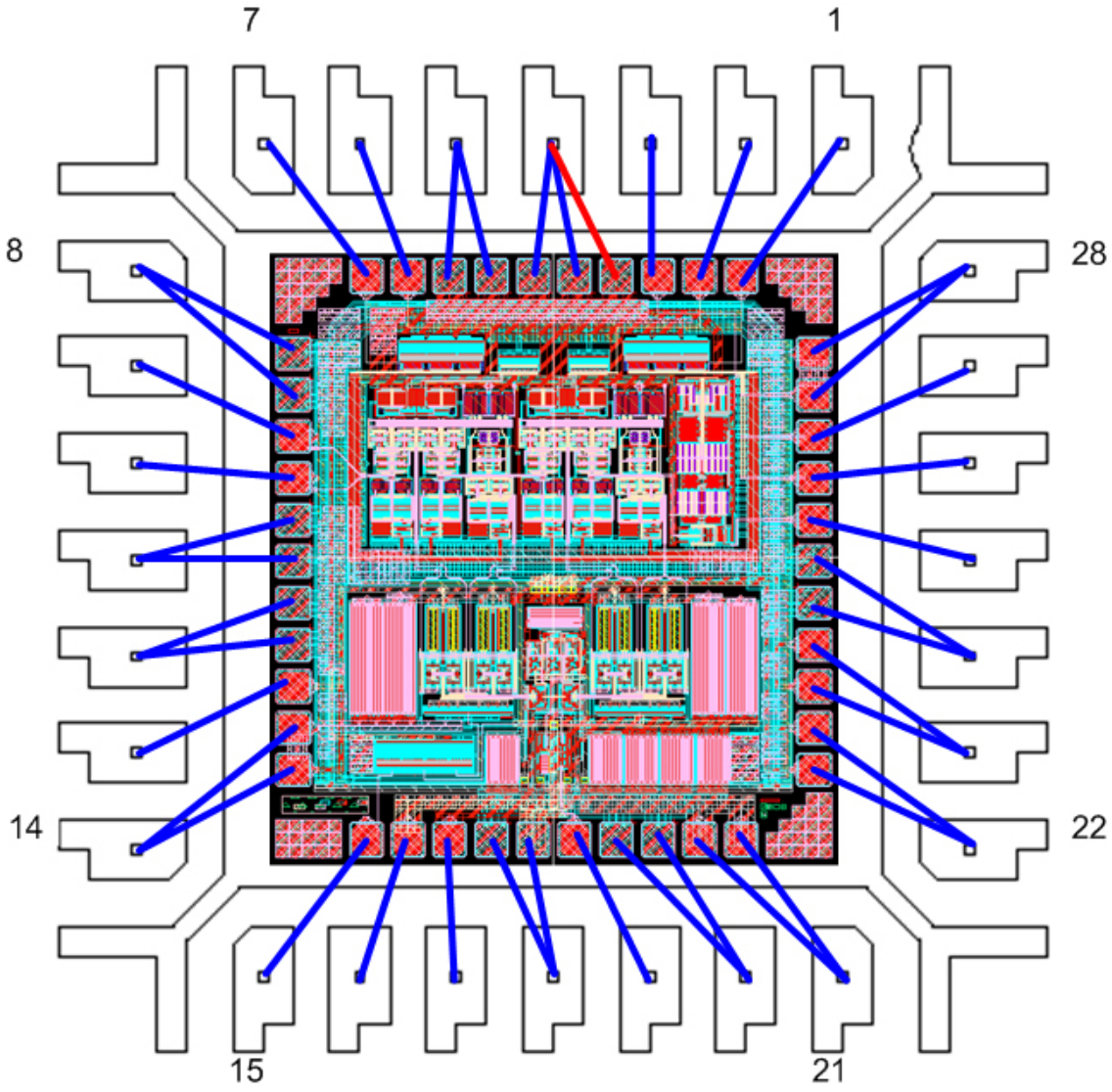


Figure 90: Bonding diagram of the second SHA chip.

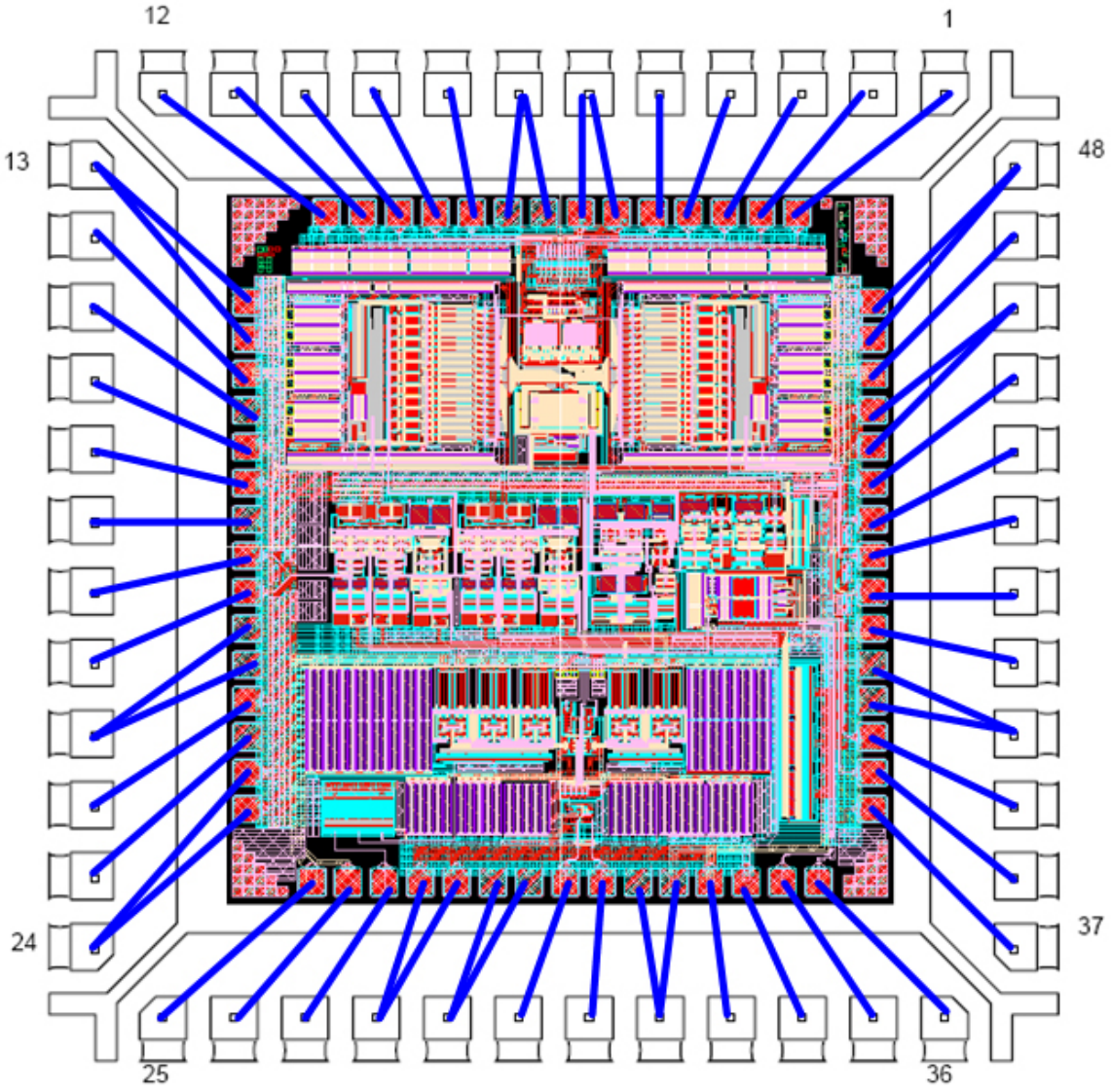


Figure 91: Bonding diagram of the ADC chip.

REFERENCES

[1] B. Razavi. *Principles of data conversion system design*. IEEE Press, New York.

[2] M. Gustavsson, J. J. Wikner, N. Tan, and N. N. Tan. *CMOS data converters for communications*. Kluwer Academic Pub., 2000.

[3] B. Razavi. Design of sample-and-hold amplifiers for high-speed low-voltage A/D converters. *Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997*, pages 59–66, 1997.

[4] B. G. Streetman. *Solid State Electronic Devices*. Prentice-Hall, Upper Saddle River, NJ, 1995.

[5] P. Vorenkamp and P. M. Verdaasdonk. Fully bipolar, 120-Msample/s 10-b track-and-hold circuit. *Solid-State Circuits, IEEE Journal of*, 27(7), 1992.

[6] A. Boni, A. Pierazzi, and C. Morandi. A 10-b 185-MS/s track-and-hold in 0.35-μ m CMOS. *Solid-State Circuits, IEEE Journal of*, 36(2):195–203, 2001.

[7] Y. T. Wang and B. Razavi. An 8-bit 150-MHz CMOS A/D converter. *Solid-State Circuits, IEEE Journal of*, 35(3):308–317, 2000.

[8] M. J. Choe, B. S. Song K., and Bacrania. An 8-b 100-MSample/s CMOS pipelined folding ADC. *Solid-State Circuits, IEEE Journal of*, 36(2):184–194, 2001.

[9] K. Y. Kim, N. Kusayanagi, and A. A. Abidi. A 10-b, 100-MS/s CMOS A/D converter. *Solid-State Circuits, IEEE Journal of*, 32(3):302–311, 1997.

[10] H. Dinc. An 8-bit current mode ripple folding A/D converter. *Masters Thesis*, 2002.

[11] H. Dinc and F. Maloberti. An 8-bit current mode ripple folding A/D converter. *Circuits and Systems, 2003. ISCAS'03. Proceedings of the 2003 International Symposium on*, 1, 2003.

[12] P. Vorenkamp and R. Roovers. A 12-b, 60-MSample/s cascaded folding and interpolating ADC. *Solid-State Circuits, IEEE Journal of*, 32(12):1876–1886, 1997.

[13] R. C. Taft, C. A. Menkus, M. R. Tursi, O. Hidri, and V. Pons. A 1.8-V 1.6-GSample/s 8-b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency. *Solid-State Circuits, IEEE Journal of*, 39(12):2107–2115, 2004.

[14] C. Sandner, M. Clara, A. Santner, T. Hartig, F. Kuttner, D. C. Villach, I. T. Austria, and A. Villach. A 6-bit 1.2-GS/s low-power flash-ADC in 0.13 μm digital CMOS. *Solid-State Circuits, IEEE Journal of*, 40(7):1499–1505, 2005.

[15] K. Uyttenhove and M. S. J. Steyaert. A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25 μm CMOS. *Solid-State Circuits, IEEE Journal of*, 38(7):1115–1122, 2003.

[16] P. C. S. Scholtens and M. Vertregt. A 6-b 1.6-Gsample/s flash ADC in 0.18 μm CMOS using averaging termination. *Solid-State Circuits, IEEE Journal of*, 37(12):1599–1609, 2002.

[17] K. Uyttenhove, A. Marques, and M. Steyaert. A 6-bit 1 GHz acquisition speed CMOS flash ADC with digital error correction. *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000*, pages 249–252, 2000.

[18] M. Choi and A. A. Abidi. A 6-b 1.3-Gsample/s A/D converter in 0.35-μm CMOS. *Solid-State Circuits, IEEE Journal of*, 36(12):1847–1858, 2001.

[19] C. Lane. A 10-bit 60 Msps flash ADC. *Bipolar Circuits and Technology Meeting, 1989., Proceedings of the 1989*, pages 44–47, 1989.

[20] C. Moreland, F. Murden, M. Elliott, J. Young, M. Hensley, and R. Stop. A 14-bit 100-Msample/s subranging ADC. *Solid-State Circuits, IEEE Journal of*, 35(12):1791–1798, 2000.

[21] M. P. Flynn and B. Sheahan. A 400-Msample/s, 6-b CMOS folding and interpolating ADC. *Solid-State Circuits, IEEE Journal of*, 33(12):1932–1938, 1998.

[22] J. van Valburg and R. J. van de Plassche. An 8-b 650-MHz folding ADC. *Solid-State Circuits, IEEE Journal of*, 27(12):1662–1666, 1992.

[23] G. Geelen and E. Paulus. An 8b 600MS/s 200mW CMOS folding A/D converter using an amplifier preset technique. *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pages 254–526, 2004.

[24] B. Hernes et al. A 1.2 V 220 MS/s 10 bit pipeline ADC implemented in 0.13 μ m digital CMOS. *IEEE Int. Solid-State Circuits Conf.(ISSCC) Dig. Tech. Papers*, pages 256–257, 2004.

[25] B. M. Min, P. Kim, F. W. Bowman, D. M. Boisvert, and A. J. Aude. A 69-mW 10-bit 80-MSample/s pipelined CMOS ADC. *Solid-State Circuits, IEEE Journal of*, 38(12):2031–2039, 2003.

[26] J. Li and U. K. Moon. A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique. *Solid-State Circuits, IEEE Journal of*, 39(9):1468–1476, 2004.

[27] E. Siragusa and I. Galton. A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC. *Solid-State Circuits, IEEE Journal of*, 39(12):2126–2138, 2004.

[28] Y. Chiu, P. R. Gray, and B. Nikolic. A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR. *Solid-State Circuits, IEEE Journal of*, 39(12):2139, 2004.

[29] K. Dyer, D. Fu, S. Lewis, and P. Hurst. Analog background calibration of a 10 b 40 Msample/s parallel pipelined ADC. *Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International*, pages 142–143, 1998.

[30] H. C. Liu, Z. M. Lee, and J. T. Wu. A 15 b 20 MS/s CMOS pipelined ADC with digital background calibration. *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pages 454–539, 2004.

[31] K. Nair and R. Harjani. A 96dB SFDR 50MS/s digitally enhanced CMOS pipeline A/D converter. *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pages 456–557, 2004.

[32] J.W. Mulder, C.M. Ward, L. Chi-Hung, D. Kruse, J. R. Westra, M. Lugthart, E. Arslan, R. J. van de Plassche, K. Bult, and F. L. M. van der Goes. A 21-mW 8-b 125-MSample/s ADC in 0.09-mm^2 0.13-μ m CMOS. *Solid-State Circuits, IEEE Journal of*, 39(12):2116–2125, 2004.

[33] B. Murmann and B. E. Boser. A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification. *Solid-State Circuits, IEEE Journal of*, 38(12):2040–2050, 2003.

[34] J. L. McCreary and P. R. Gray. All-MOS charge redistribution analog-to-digital conversion techniques part: I. *Solid-State Circuits, IEEE Journal of*, 10(6):371–379, 1975.

[35] D. Fu, K. C. Dyer, S. H. Lewis, and P. J. Hurst. A digital background calibration technique for time-interleaved analog-to-digital converters. *Solid-State Circuits, IEEE Journal of*, 33(12):1904–1911, 1998.

[36] B. Murmann. A/D converter trends: Power dissipation, scaling and digitally assisted architectures. *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pages 105 –112, sep. 2008.

[37] B. Murmann. A/D converter trends: Power dissipation, scaling and digitally assisted architectures. *[Online].Available: http://www.stanford.edu/ murmann/adcsurvey.html*.

[38] W. Yang, D. Kelly, L. Mehr, M. T. Sayuk, and L. Singer. A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input. *Solid-State Circuits, IEEE Journal of*, 36(12):1931–1936, 2001.

[39] A. Panigada and I. Galton. A 130 mW 100 MS/s pipelined ADC with 69 dB SNDR enabled by digital harmonic distortion correction. *Solid-State Circuits, IEEE Journal of*, 44(12):3314–3328, dec. 2009.

[40] A. M. A. Ali, A. S. Morgan, and S. G. Bardsley. Correlation-based background calibration of pipelined converters with reduced power penalty, August 2010.

[41] C. R. Grace, P. J. Hurst, and S. H. Lewis. A 12 b 80 MS/s pipelined ADC with bootstrapped digital calibration. *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pages 460–539, 2004.

[42] Ahmed Mohamed Abdelatty Ali. Analog-to-digital converter methods and structures for interleavably processing data signals and calibration signals, January 2005.

[43] J. C. Jensen and L. E. Larson. A Broadband 10-GHz track-and-hold in Si/SiGe HBT technology. *Solid-State Circuits, IEEE Journal of*, 36(3):325, 2001.

[44] R. Payne, M. Corsi, D. Smith, S. Kaylor, and D. Hsieh. A 16b 100-to-160MS/s SiGe BiCMOS pipelined ADC with 100dBFS SFDR. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, pages 294 –295, 2010.

[45] A. Razzaghi and M. C. F. Chang. A 10-b, 1-GSample/s track-and-hold amplifier using SiGe BiCMOS technology. *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003*, pages 433–436, 2003.

[46] A. N. Karanicolas. A 2.7-V 300-MS/s track-and-hold amplifier. *Solid-State Circuits, IEEE Journal of*, 32(12):1961–1967, 1997.

[47] T. Baumheinrich, B. Pregardier, and U. Langmann. A 1-GSample/s 10-b full Nyquist silicon bipolar track & hold IC. *Solid-State Circuits, IEEE Journal of*, 32(12):1951–1960, 1997.

[48] H. Dinc and P.E. Allen. A 1.2 GSample/s double-switching CMOS THA with 62 dB THD. *Solid-State Circuits, IEEE Journal of*, 44(3):848 –861, mar. 2009.

[49] P Wambacq and W Sansen. *Distortion Analysis of Analog Integrated Circuits*. Kluwer Academic Publishers, Norwell, MA, USA, 1998.

[50] A. van den Bosch, M. A. F. Borremans, M. S. J. Steyaert, and W. Sansen. A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter. *Solid-State Circuits, IEEE Journal of*, 36(3):315–324, 2001.

[51] M. Wingender and N. Chantier. 3 GS/s S-Band 10 Bit ADC and 12 Bit DAC on SiGeC technology. *Radar Conference - Surveillance for a Safer World, 2009. RADAR. International*, pages 1 –6, oct. 2009.

[52] C. Fiocchi, U. Gatti, and F. Maloberti. A 10 b 250 MHz BiCMOS track and hold. *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC., 1997 IEEE International*, pages 144–145, 1997.

[53] B. Pregardier, U. Langmann, and WJ Hillery. A 1.2-GS/s 8-b silicon bipolar track & hold IC. *Solid-State Circuits, IEEE Journal of*, 31(9):1336–1339, 1996.

[54] S.H. Lewis. Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications. *Circuits and Systems II, IEEE Transactions on*, 39(8):516–523, 1992.

[55] B. Razavi. *Design of analog CMOS integrated circuits*. McGraw-Hill, 2000.

[56] P.E. Allen and R.D. Holberg. *CMOS analog circuit design*. Oxford University Press, 2002.

[57] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer. *Analysis and design of analog integrated circuits*. Wiley, 2001.

[58] K. Kattmann and J. Barrow. A technique for reducing differential non-linearity errors in flash A/D converters. In *Solid-State Circuits Conference, 1991. Digest of Technical Papers. 38th ISSCC., 1991 IEEE International*, pages 170 –171, February 1991.

[59] P.M. Figueiredo and J.C. Vital. Kickback noise reduction techniques for CMOS latched comparators. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 53(7):541 – 545, jul. 2006.

[60] B.-S. Song, S.-H. Lee, and M.F. Tompsett. A 10-b 15-MHz CMOS recycling two-step A/D converter. *Solid-State Circuits, IEEE Journal of*, 25(6):1328–1338, dec. 1990.

[61] Chi-Hung Lin and K. Bult. A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2. *Solid-State Circuits, IEEE Journal of*, 33(12):1948 –1958, dec. 1998.

[62] A. Van den Bosch, M. Steyaert, and W. Sansen. An accurate statistical yield model for CMOS current-steering D/A converters. *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, 4:105–108, 2000.

[63] M.J.M. Pelgrom, A.C.J. Duinmaijer, and A.P.G. Welbers. Matching properties of MOS transistors. *Solid-State Circuits, IEEE Journal of*, 24(5):1433–1440, dec. 1989.

[64] A. Hastings. *The art of analog layout*. Prentice Hall, 2005.

[65] J. Yuan and C. Svensson. New single-clock CMOS latches and flipflops with improved speed and power savings. *Solid-State Circuits, IEEE Journal of*, 32(1):62–69, 1997.

[66] A. Ali, A. Morgan, C. Dillon, G. Patterson, S. Puckett, P. Bhoraskar, and H. Dinc. A 16-Bit 250-MS/s IF sampling pipelined ADC with background calibration. *Solid-State Circuits, IEEE Journal of*, 12, dec. 2010.

[67] R.C. Taft, P.A. Francese, M.R. Tursi, O. Hidri, A. MacKenzie, T. Hoehn, P. Schmitz, H. Werker, and A. Glenny. A 1.8V 1.0GS/s 10b self-calibrating unified-folding-interpolating ADC with 9.1 ENOB at Nyquist frequency. 44(12):3294–3304, 2009.

[68] Wei An and C.A.T. Salama. An 8-bit, 1-Gsample/s folding-interpolating analog-to-digital converter. In *Solid-State Circuits Conference, 2000. ESSCIRC '00. Proceedings of the 26th European*, pages 228 – 231, 2000.

[69] F. Vessal and Salama C.A.T. An 8-bit 2-Gsample/s folding-interpolating analog-to-digital converter in SiGe technology. *Solid-State Circuits, IEEE Journal of*, 39(1):238 –241, January 2004.

[70] D.-L. Shen and T.-C. Lee. A 6-bit 800-MS/s Pipelined A/D Converter With Open-Loop Amplifiers. *Solid-State Circuits, IEEE Journal of*, 42(2):258 –268, 2007.

[71] K. Bult and G.J.G.M. Geelen. A fast-settling CMOS op amp for SC circuits with 90-dB DC gain. *Solid-State Circuits, IEEE Journal of*, 25(6):1379 –1384, December 1990.

[72] B. Murmann and B.E. Boser. *Digitally assisted pipeline ADCs: Theory and implementation*. Springer, 2004.

[73] K. Bult. Analog design in deep sub-micron CMOS. In *Solid-State Circuits Conference, 2000. ESSCIRC '00. Proceedings of the 26th European*, pages 126 – 132, 2000.

[74] K. Uyttenhove and M.S.J. Steyaert. Speed-power-accuracy tradeoff in high-speed CMOS ADCs. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 49(4):280 –287, April 2002.

[75] Crystal Semiconductor. Application Note 30.

[76] H. Dinc, S. Chuang, P.E. Allen, and P. Hasler. A rail to rail, slew-boosted precharge buffer. *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, page 4 pp., 2006.

[77] F. Behbahani, A. Karimi-Sanjaani, Wee-Guan Tan, A. Roithmeier, J.C. Leete, K. Hoshino, and A.A. Abidi. Adaptive analog IF signal processor for a wide-band CMOS wireless receiver. *Solid-State Circuits, IEEE Journal of*, 36(8):1205 –1217, aug. 2001.

[78] H. Dinc, P.E. Allen, and S. Chakraborty. A low distortion, current feedback, programmable gain amplifier. *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pages 4819 – 4822 Vol. 5, may. 2005.

[79] S. Yan and E. S. Sinencio. Low voltage analog circuit design techniques: A tutorial. *Fundamentals of Electronics, Communications and Computer Sciences, IEICE Transactions*, E83-A(2):179–196, 2000.

[80] A.I.A. Cunha, M.C. Schneider, and C. Galup-Montoro. An MOS transistor model for analog circuit design. *Solid-State Circuits, IEEE Journal of*, 33(10):1510 – 1519, oct. 1998.

[81] S. Franco. Analytical foundations of current-feedback amplifiers. *Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on*, 2:1050–1053, may. 1993.

[82] E. Iroaga and B. Murmann. A 12-Bit 75-MS/s pipelined ADC using incomplete settling. *Solid-State Circuits, IEEE Journal of*, 42(4):748 –756, 2007.

[83] D. Y. Aksin and F. Maloberti. Very high-speed bjt buffer for track-and-hold amplifiers with enhanced linearity. In *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*.